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Representation of the temperature nano-sensors via cylindrical gate-all-around Si-NW-FET

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ABSTRACT

In this paper, the temperature dependence of some characteristics of cylindrical gate-all-around Si nanowire field effect transistor (GAA-Si-NWFET) is investigated to representing the temperature nano-sensor structures and improving their performance. Firstly, we calculate the temperature sensitivity of drain-source current versus the gate-source voltage of GAA-Si-NWFET to propose the temperature nano-sensor circuit. Then the solutions of increasing current temperature sensitivity are discussed by investigating the effects of the oxide thickness and the channel diameter on this parameter. Secondly, in this study, we demonstrate the temperature dependence of the transconductance (g_m) and output resistance (r_o) of the GAA-Si-NWFET. We have proposed the amplifier circuit as a temperature sensor based on the temperature dependence of these parameters. In addition, we have changed the channel diameter and the oxide thickness to increase the temperature sensitivity of g_m and subsequently, temperature sensitivity of proposed sensor. Ultimately, the effects of channel diameter and oxide thickness on the temperature sensitivity of g_m will be analytically investigated.

Keywords: *Semiconductor nanowire field effect transistor; Transconductance; Output resistance; Temperature sensitivity; Temperature nano-sensor.*

INTRODUCTION

Silicon nanowire field effect transistors (Si-NW-FETs) have drawn lots of attention in recent years [1, 2]. These transistors are one of the promising candidates for further reducing the size of the devices and the type of cylindrical, with gate all around (GAA) due to the efficient gate controllability, is excellent [3]. This device has several applications, which can note temperature sensor manufacturing [4].

In [4] the temperature dependence for characteristics of Si-NW-FETs such as subthreshold swing (*SS*), the ON-OFF current ratio (I_{ON}/I_{OFF}) has been reported. In [5], the temperature dependence for drain-source (I_{DS}) versus gate-source voltage (V_{GS}) in the temperature range of 0 to 25°C, sub-threshold swing and the I_{ON}/I_{OFF} ratio of Si-NW-FETs has been investigated. In [6], the *I-V* characteristic of Si-NW-FET as a temperature sensor in the temperature range of 0 to 100°C has been evaluated. Furthermore, the effect of temperature on the drain Induced Barrier Lowering (*DIBL*) of Si-NW-FET [7], and designing, Manufacturing, and characteristics of the transistor based temperature sensors [2, 8-12] have been investigated. According to these studies, the temperature nano-sensor structures based on the cylindrical GAA-Si-NW-FET and theoretical schemes to increase their temperature sensitivity have been less studied.

In this paper, we have investigated the temperature dependence of the characteristics of cylindrical GAA-Si-NW-FET, such as I_{DS} and transconductance by using a model proposed by Sedigh *et al.* [13]. Base on the simulation results we have proposed the temperature nano-sensor structures and demonstrated the techniques of increasing temperature sensitivity such as channel diameter and oxide thickness variation as solutions to improve the performance of these sensors. In addition, the similarity of the simulation results and the analytical models has been demonstrated.

In this paper, in Sec. 2, device structure and simulation model are introduced. Section 3 is illustrated to the simulation results and discussions. We conclude this paper in Sec. 4

EXPERIMENTAL

A schematic representation of cylindrical GAA-Si-NW-FET is demonstrated in Figure 1. The channel length and diameter are L_{ch}= 10 nm and d_{ch} = 2.75 nm, respectively. The channel is covered by a layer of SiO_2 of thickness d_{ox} = 1 nm.

We have studied the temperature effect on the characteristics of cylindrical GAA-Si-NW-FET by using a model proposed by Sedigh *et al.*[13]. Figure 2 shows the $I_{DS} - V_{GS}$ characteristics of cylindrical GAA-Si-NW-FET of Figure 1, for V_{DS} = 0.4 V at temperatures of 300, 250, 200, 150, 100, and 50 K. The curves of I_{DS} versus V_{GS} are similar to the I_{DS}–V_{GS} characteristics calculated in the reference [13].

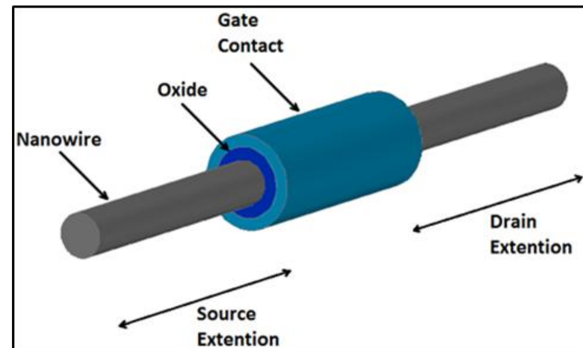

Fig. 1. The schematic of cylindrical GAA-Si-NW-FET. The channel length and diameter are L_{ch}= 10 nm and d_{ch}= 2.75 nm, respectively, and d_{ox} = 1 nm.

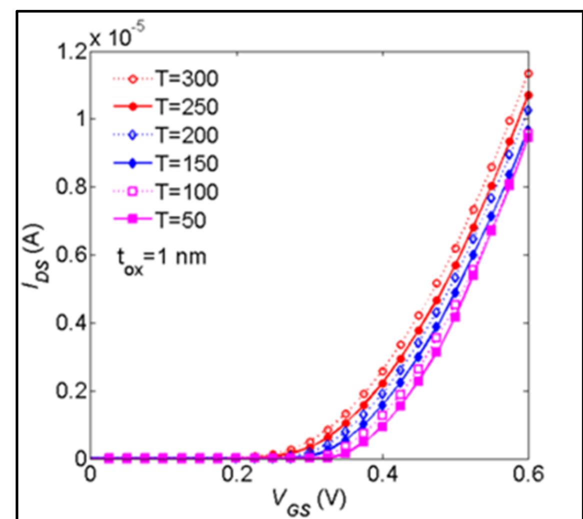

Fig. 2. The I_{DS} - V_{GS} characteristics of the structure of Fig. 1 with channel diameter 2.75 nm, and oxide thickness 1 nm under V_{DS} = 0.4 V at different temperatures, *T* = 50, 100, 150, 200, 250 and 300 K.

RESULTS AND DISCUSSION

Figure 2 shows that as the temperature decreases the drain-source current also decreases. Based on this behavior, the aim of our research is to provide a discussion regarding the use of this device as a temperature sensor. Also in Figure 2 it can be seen that in the V_{GS} greater than 0.5 V the temperature dependence of I_{DS} is less in low temperature compared to high temperature. To

investigate this behavior, for a given V_{GS}, the I_{DS} temperature sensitivity parameter is calculated as follows [13]

$$S= (\partial I_{DS})/\partial T \qquad (1)$$

Figure 3 is shown the temperature sensitivity extracted from Figure 2. As the S increases at the range of gate source voltage 0-0.5 V and its maximum value is S = 8.054 nA/K. Therefore, a special attention to the V_{GS} is needed to achieve more temperature sensitivity of $I_{DS.}$ Accordingly, the temperature sensor of Figure 4 is proposed. Furthermore, we investigate the effect of oxide thickness and channel diameter, as two solutions to improve the performance of this proposed sensor.

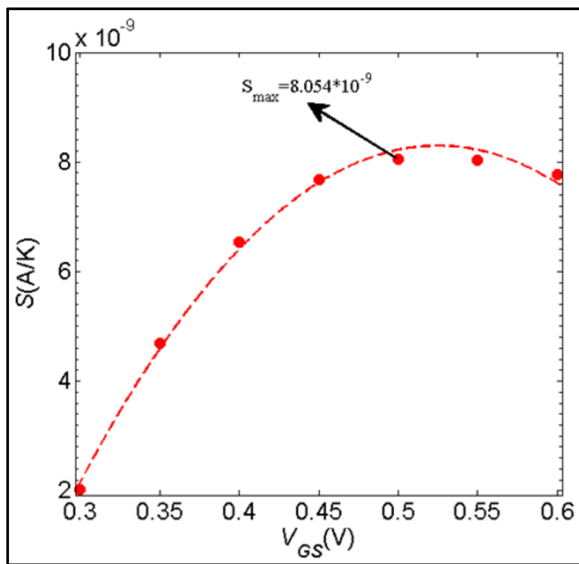

Fig. 3. The drain-source current temperature sensitivity versus V_{GS} extracted from Fig. 2 for d_{ch} = 2.75nm and d_{ox} = 1nm at V_{DS}= 0.4 V.

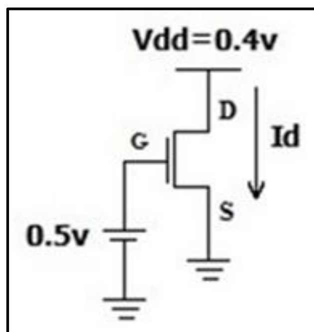

Fig. 4. The proposed temperature sensor circuit using the Si-NW-FET of Fig. 1.

Figure 5 shows the current temperature sensitivity versus the V_{GS} for d_{ch} = 2.75 nm and the oxide thickness of 0.5 and 2 nm biased under V_{DS} = 0.4 V. In this figure it can be seen that the S decreases for d_{ox}=0.5 nm and V_{GS} more than 0.4 V. The maximum value of current temperature sensitivity (S_{max}) is 7.605 nA/K for d_{ox} = 0.5 nm at V_{GS} = 0.4 V. For V_{GS} = 0.6 V, as d_{ox} increases to 2 nm, the S_{max} also increases to 8.977 nK/A.In this figure by increasing the oxide thickness, the gate control on the channel is decreased, therefore the temperature sensitivity of drain-source current is increased. Another strategy to improve the performance of the sensor represented in Figure 4 changes the channel diameter of the Si-NW-FET. Accordingly, we calculate the S for d_{ch}= 1, 2 and 2.75 nm that are shown in Figure 6. This figure illustrates in the range of V_{GS} from 0 to 0.55 V the maximum value of S is attained at d_{ch}= 2.75 nm. In this figure by increasing the channel diameter, according to Ref. 13 the temperature sensitivity of electron effective mass and hence, the temperature sensitivity of drain-source current is increased.

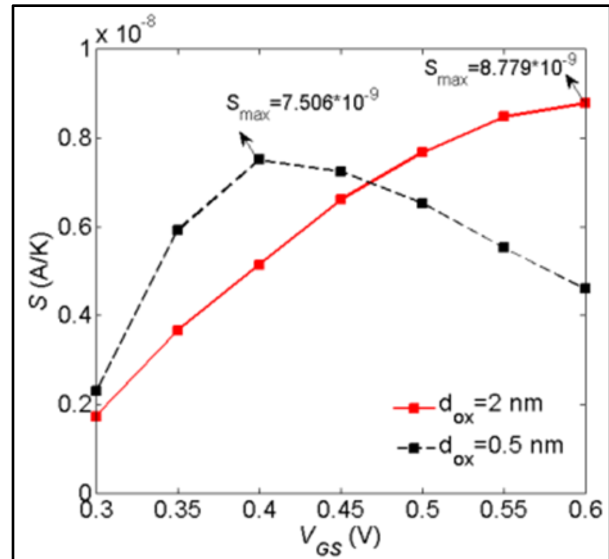

Fig. 5. The S versus V_{GS} for d_{ch} = 2.75 nm, d_{ox}= 0.5 and 2 nm at V_{DS} = 0.4 V.

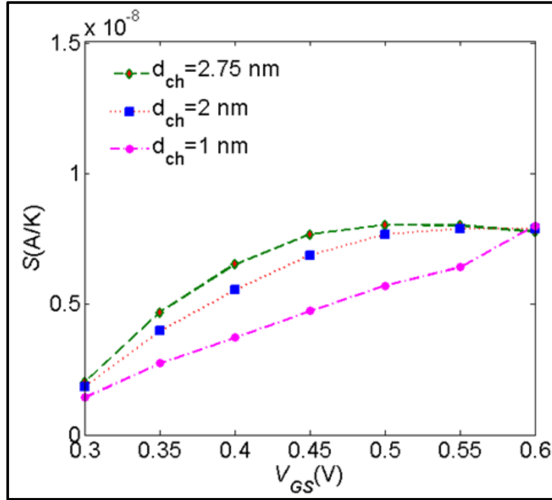

Fig. 6. The S versus V_{GS} of transistor as illustrated in Fig. 1 for d_{ox} = 1 nm, various channel diameters d_{ch} = 1, 2 and 2.75 nm at V_{DS} = 0.4 V.

Furthermore, we investigate the temperature sensitivity of transconductance (g_m) of Si-NW-FET illustrated in Figure 1. The g_m is calculated by the following expression and the I_{DS}-V_{GS} characteristics of Figure 2.

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}} \quad (2)$$

Consequently, we have calculated the g_m versus temperature for d_{ox}= 1 nm and d_{ch}= 2.75 nm at V_{GS}= 0.35 V and V_{DS}= 0.4 V and it is shown in Figure 7.

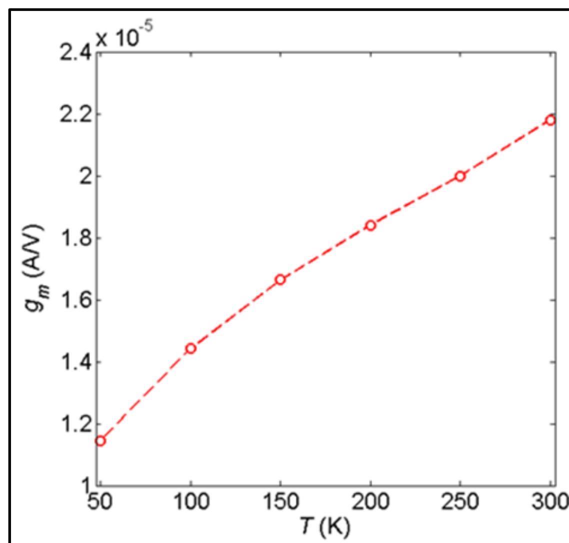

Fig. 7. The temperature dependence of g_m of transistor as illustrated in Fig. 1 for d_{ox} = 1 nm, d_{ch} = 2.75 nm at V_{DS} = 0.4 V.

On the other hand, the temperature dependence of g_m has been investigated based on analytical model. The drain-source current of Si-NW-FET is given by [14]

$$I_{DS} = wC_{ox}v_T(V_{GS} - V_{th}) \quad (3)$$

Where w is channel width, V_{th} threshold voltage and v_T being carrier average velocity that is given by v_T = $[2kT/\pi m^*]^{0.5}$ in which m^* is electron effective mass and k is the Boltzmann constant and C_{ox} is oxide capacitor which is expressed by [1]

$$C_{ox} = \frac{2\pi\varepsilon_0\varepsilon_r}{ln\left(\frac{d_{ch}+2d_{ox}}{d_{ch}}\right)} \quad (4)$$

Where d_{ch} is the channel diameter, d_{ox} is the oxide thickness, ε_0 and ε_r are the permittivity of the free space and silicon, respectively. We calculate transconductance relationship of this transistor, according to (3) and (4). It is presented as follows:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = wC_{ox}v_T = wC_{ox}\sqrt{\frac{2kT}{\pi m^*}} \quad (5)$$

As temperature decreases, the electron effective mass increases [13], so based on the (5) the g_m also decreases. This behavior is similar to the temperature dependence of g_m calculated by simulation, which is illustrated in Figure 7. Therefore, environmental temperature can be measured by the use of temperature dependence of the transconductance. Accordingly the circuit illustrated in Figure 8 as a temperature sensor is proposed. In this amplifier circuit the input signal and output signal are v_{reff} and v_{out}, respectively. The gain of the circuit is given as follows:

$$A_v = \frac{v_{out}}{v_{reff}} = -g_m(\mathrm{R}\|\mathrm{r}_0) \quad (6)$$

Where R is load resistance and r_o is output resistance of the transistor which is shown in Figure 1. The temperature dependence of r_o is illustrated in Figure 8. This figure also shows an excellent match of the extracted data and the formula represented by r_o (T)≈ $1.87\times10^{-5}T^2$–0.011T+2.84. The Figure 7 and Figure 8 demonstrate that as temperature decreases, the transconductance and the output resistance decreases and increases, respectively. So according to (6), by selecting a small value for the load

resistance, the temperature dependence of r_o can be almost neglected. Assuming the R and $v_{reff,}$ are temperature independent, the temperature dependence of output voltage proportional to the temperature dependence of the g_m.

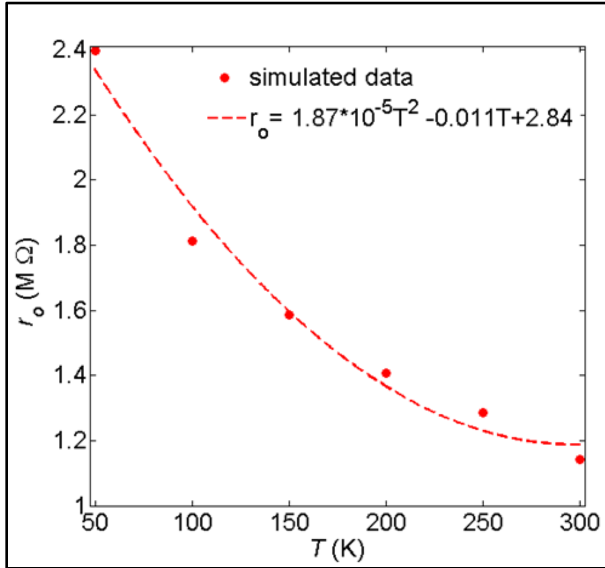

Fig. 8. The temperature dependence of output resistant of device illustrated in Fig. 1. Dashed line represents the quadratic fit.

We have studied the temperature dependence of g_m for various values of d_{ox} as a solution to improve performance of the temperature sensor of Figure 9. The transconductance versus temperature plotted for d_{ch}= 2.75 nm and the various oxide thickness of 0.5, 1, and 2 nm are shown in Figure 10. This figure shows that for a given temperature, a decrease in the oxide thickness lead to an increase in the transconductance. This figure also illustrates the temperature sensitivity of g_m for a given d_{ch}, increases with decreasing the oxide thickness. On the other hand, we have investigated the effects of oxide thickness on the temperature dependence of g_m based on analytical model. Expressions (4) and (5) indicate that for a given temperature, a decrease in the oxide thickness lead to an increase in the oxide capacitance and subsequently an increase in the transconductance. Moreover, we calculate the temperature sensitivity relationship of g_m from expression (5) and is shown in expression (7). Based on this expression the g_m temperature sensitivity increases with decreasing the oxide thickness. These behaviors are similar to the simulation results illustrated in Figure 10. This figure also shows an excellent match of the extracted data with the formulas at various oxide thickness, d_{ox}= 0.5, 1 and 2 nm.

$$\frac{\partial g_m}{\partial T} = w\frac{2\pi\varepsilon_0\varepsilon_r}{ln\left(\frac{d_{ch}+2d_{ox}}{d_{ch}}\right)}\sqrt{\frac{2k}{\pi m^*}}\frac{1}{2\sqrt{T}} \qquad (7)$$

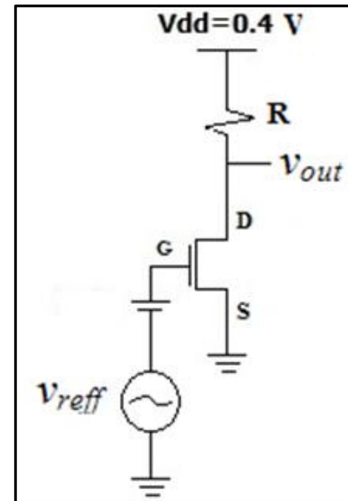

Fig. 9. The proposed circuit as a temperature sensor by the cylindrical GAA-Si-NWFET of fig. 1.

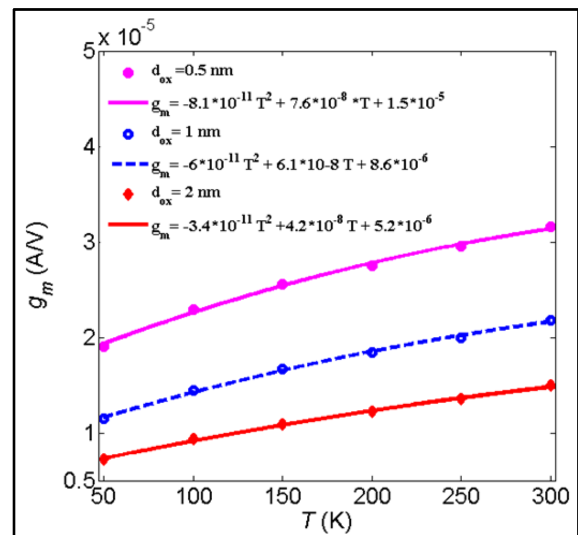

Fig. 10. The transconductance versus temperature for d_{ch}= 2.75 nm and various oxide thicknesses, d_{ox}= 0.5, 1, and 2 nm. Solid and dashed lines represent the quadratic fit.

Figure 11 shows the transconductance plotted versus temperature for d_{ch}=1, 2 and 2.75 nm

and d_{ox}= 1nm. A decrease in the channel diameter leads to an increase in the g_m at constant temperature. This behavior can be investigated by analytical expression (5). By increasing the channel diameter based on the expression (4) the oxide capacitance increases and according to the reference [15] the electron effective mass decreases, thus the g_m increases. Moreover, in Figure 11, it can be indicated that for d_{ox}= 1 nm, as the channel diameter increases, the temperature sensitivity of g_m increases. This figure also shows an excellent match of the extracted data with the formulas at various channel diameters, d_{ch}= 1, 2 and 2.75 nm. Froman analytical standpoint, it is seen that by increasing the channel diameter, the oxide capacitance and the electron effective mass increases and decreases [15], respectively. Thus, based on the analytical expression (7) the g_m increases.

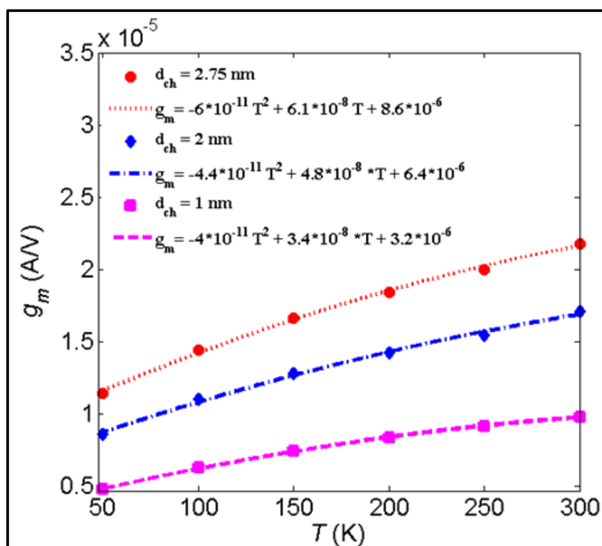

Fig. 11. The transconductance versus temperature for V_{DS}= 0.4 V at the oxide thickness of 1 nm and various channel diameters d_{ch}= 1, 2 and 2.75 nm. Dotted, dashed and dashed-dotted lines represent the quadratic fit.

CONCLUSIONS

In this paper, we have proposed the temperature nano-sensor structures based on the cylindrical gate-all-around Si-NW-FET and improved their performance. The temperature sensor circuit is proposed by connecting the gate to supply voltage more than the V_{DS} for reaching to the highest temperature sensitivity. Moreover, it is observed that as the oxide thickness and the channel diameter increase, the temperature sensitivity of I_{DS} increases. Furthermore, we have calculated the temperature dependence of transconductance of the Si-NW-FET shown in figure 1 and realized that as temperature decreases, the g_m also decreases. According to the temperature dependence of g_m, the amplifier circuit is proposed as a temperature sensor. We have also observed that in this circuit by any increase in temperature, the g_m and the output resistance increases and decreases, respectively. Thus, we have assumed that the R and v_{reff} are temperature independent and the value of R is less than the minimum value of r_o. Eventually, we have numerical studied the effects of oxide thickness and channel diameter on the temperature dependence of the g_m and its temperature sensitivity. We have recognized that by increasing in the oxide thickness and the channel diameter, the temperature sensitivity of g_m also increases.

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