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ORIGINAL ARTICLE

Gate structural engineering of MOS-like junctionless Carbon nanotube field effect transistor (MOS-like J-CNTFET)

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Abstract

In this article, a new structure is presented for MOS (Metal Oxide Semiconductor)-like junctionless carbon nanotube field effect transistor (MOS-like J-CNTFET), in which dual material gate with different work-functions are used. In the aforementioned structure, the size of the gates near the source and the drain are 14 and 6 nm, respectively, and the work-functions are equal and 0.5 eV less than the work-function of the intrinsic carbon nanotube. The simulation is carried out in the ballistic regime using the non-equilibrium Green's function (NEGF) in the mode space approach. The simulation results show that the proposed structure has a better am-bipolar behavior and less OFF current compared to a conventional junctionless structure with the same dimensions. In the new structure, the hot carrier effect is also reduced due to the reduced electric field near the drain, and with regard to a peak in the electric field curve at the junction of two gates, the gate control on the channel will be increased.

Keywords: *Carbon Nanotubes (CNTs); Drain Induced Barrier Lowering (DIBL); Field Effect Transistor (FET); Junctionless; Non-Equilibrium Green's Function (NEGF).*

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INTRODUCTION

Silicon devices have been highly popular in the past several decades due to proper scalability properties [1-2]. By miniaturizing the technology dimensions and reaching to the nanoscale dimensions, these devices have many physical limitations [3]. Thus, many attempts have been made to introduce a new element instead of silicon, which can be produced in such dimensions. Graphene is one of these materials [4–6], which offers benefits from high strength, and appropriate electrical, mechanical and optical properties, but because the energy-gap is equal to zero, it cannot be used in the channel of the field effect transistors. In order to create the energy-gap in the structure, the graphene layers can be easily patterned to the carbon nanotubes using the existing manufacturing technology methods [7, 8]. The carbon nanotubes have nearly ballistic properties, and due to the high saturation speed and electron mobility, are good candidates for the channel of field effect transistors. Carbon Nano Tube Field Effect Transistor (CNTFETs) can be used in many other applications [9]. The single-walled carbon nanotubes have one-dimensional nature, high structural quality as well as small diameter, which can lead to the excellent control by the gate electrode [10, 11]. Drain induced barrier lowering (DIBL) is one of the short-channel effects in MOSFETs, which reduces the transistor threshold voltage by increasing the drain voltage. For more decrease in this effect as well as other short-channel effects, and reaching a higher transconductance and better control on charge carriers in the channel, the researchers proposed the double gate transistors (DG-MOSFET) [12, 13] and analyze the effects of oxide thickness (tox.

Because of needing to extremely sharp doping profile for nanometer-sized junctions in MOSFETs, forming the p-n junctions is very difficult and cause serious challenges such as short-channel effects. Furthermore, random effects due to the

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location of impure atoms mean that p-n junctions cannot be well realized in nanometer dimensions. Junctionless field effect transistors have been introduced to overcome these problems, due to the lack of existing any junction.

The junctionless transistors have many advantages including reduced short channel effects such as steeper sub-threshold swing and less DIBL compared to the conventional MOSFETs [14]. The junctionless double gate MOSFETs have the structure of common double gate MOSFETs, but there is a difference that channel is also doped the same as source and drain. As a result, in contrast to the conventional double gate MOSFETs, there is no junction between source-channel and drain-channel. Hence, such structures are called junctionless. The junctionless transistors have special advantages in terms of manufacturing process and device performance [15, 16].

To enhance the immunity against short channel effects, a structure called dual material gate (DMG) MOSFET was proposed [17]. In the above structure, a spacer with high gate dielectric and different work-functions are used. In terms of design, the above structure has higher I_{ON}/I_{OFF} current ratio, better transconductance (G_m), lower short channel effects, and lower DIBL [18]. The other studies conducted in the performance analysis of junctionless transistors included the temperature dependence of the electrical characteristics [19, 20] strain effects on the characteristics of junctionless transistors with ballistic nature along the channel [21].

In most of the studies, the material that is used had been silicon. This article looks for structural engineering of Metal Oxide Semiconductor junctionless carbon nanotube field effect transistor (MOS-like J-CNTFET). Hence, a new structure is proposed where the dual material gate with different work-functions are used. The proposed structure specifications are compared with a conventional junctionless carbon nanotube field effect transistor with the same dimensions.

The remainder of the paper is organized as follows. In Section 2, the proposed and the conventional structures are introduced, and simulation method will be explained. In Section 3, the simulation results will be discussed and studied. Section 4 concludes the paper.

Proposed structure and computational method

In this section, the proposed and the conventional structure will be introduced. Fig. 1 (a) and (b) show the conventional and the new structure, respectively. The carbon nanotube used in both structures is selected with the same type of zigzag with n=13. Insulating gate dielectric layers are made of 2-nm thick HfO_2 with the relative dielectric constant of ε_{OX}=16. The length of source, drain and channel have been considered 10, 20 and 10 nm, respectively, and all regions have 0.0087 dopant per atom (N_{SD}=0.0087) concentration. In the new structure (Fig. 1 (b)), the gate is divided into two parts. The left gate (G_1) is close to the source region with a work-function equal to nanotube work-function ($\varphi_{CNT} = \varphi_{M1}$) and the length of 14 nm, and the right gate (G_2) is close to the drain with the length of 6-nm with a work-function of 0.5 eV lower than the work-function G1 ($\varphi_{M2} = \varphi_{M1} - 0.5$). It will also be explained how the above values will be chosen. Since in the proposed structure, the dual material gate is used, the above structure is named dual material gate junctionless carbon nano tube field effect transistor (DMG-J-CNTFET).

As the electronic devices scaling reaches to nanometer, the validity of conventional modeling methods become questionable. The simulation methods used for nanoscale devices should consider quantum mechanical effects. As mentioned earlier, the carbon nanotubes can be patterned by rolling a graphene sheet with typical diameters of 1-2 nm, and with regard to rolling a graphene sheet (according to the chirality) it can be treated as metal or semiconductor [22]. The semiconductor nanotubes are appropriate for use as the channel material of the transistors. In order to support the modeling of CNTFETs, a strong quantum limit around the nanotube in circumferential direction, quantum tunneling through the Schottky barrier in metal-nanotube contacts, quantum tunneling effect and reflection on barrier in the channel should be considered. Non-equilibrium Green's function method (NEGF), which solves the Schrödinger equation under non-equilibrium conditions and its function is based on coupling between contacts and dispersion process, provides a basis for simulation of quantum devices [23–25]. In this section, we provide a summary of NEGF simulation method.

Fig. 2 shows a general transistor that describes some of the terms used in the NEGF approach [26]. The first step is to identify an appropriate basis functions and the Hamiltonian matrix for

the channel. The self-consistence potential, as a part of Hamiltonian matrix, is included at this stage. The second step is calculation of self-energy matrices $\sum_1$, $\sum_2$, $\sum_S$, describing how a ballistic channel is coupled with source-drain contacts and the scattering process. (For simplicity, only the ballistic transport is examined ($\sum_S$=0)). After determining the Hamiltonian matrix and the self-energies, the third step is calculation of the retarded Green's function.

$$G(E)=[(E+i0^{+})I-H-\sum_1-\sum_2]^{-1} \quad (1)$$

The fourth step is to determine the relevant physical values of the Green's function.

In the ballistic limit, the existing states in the device can be divided in two sections: 1) the states filled by the carriers from the source contact that follow the source Fermi level and 2) the states filled by the drain contact that follow the drain Fermi level. The local density of states (LDOS) filled by source (drain) is equal to $D_{S(D)}=G\Gamma_{S(D)}G^{+}$ where $\Gamma_{S(D)}=i(\sum_{1(2)}-\sum^{+}_{1(2)})$ shows the energy level broadening by the source (drain). The charge density within the device is calculated through integration of local density of states (LDOS). The calculated charge density in the source is provided by equation (2).

$$Q_S(z)=(-e)\int_{E_N}^{+\infty} D_S(E,z)f(E-E_{FS})dE + e\int_{-\infty}^{E_N} D_S(E,z)\{1-f(E-E_{FS})\}dE \quad (2)$$

where e is the electron charge, and E_N is the neutral state [26]. The total charge is calculated through equation (3).

$$Q(z)=Q_S(z)+Q_D(z)=(-e)\int_{-\infty}^{+\infty} dE\,.\,\mathrm{sgn}[E-E_N(z)]\{D_S(E,z)f(\mathrm{sgn}[E-E_N(z)](E-E_{FS}))+D_D(E,z)f(\mathrm{sgn}[E-E_N(z)](E-E_{FD}))\} \quad (3)$$

where sgn(E) is the sign function, and $E_{FS(D)}$ is the source (drain) Fermi level. In a self-consistence procedure, the NEGF and Poisson's equations should be solved self-consistently for achieving the convergence, and then the drain-source current is calculated through equation (4).

$$I=\frac{4e}{h}\int T(E)\,[f_S(E)-f_D(E)]dE \quad (4)$$

where $T(E)=Trace(\Gamma_1 G\Gamma_2 G^{+})$ is the possibility of passing carriers from the source to the drain, and the additional factor 2 is related to degeneracy in the band structure of carbon nanotube.

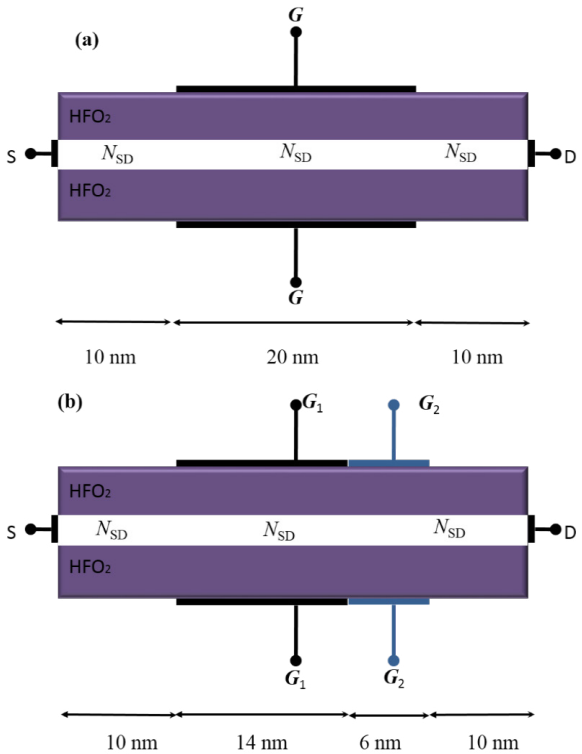

Fig. 1: The schematic view of (a) conventional MOS-like junctionless carbon nanotube field effect transistor (MOS-like J-CNTFET) (b) the proposed structure (DMG-J-CNTFET).

As shown in Fig. 2, the method starts with an initial guess for the channel potential and then the charge density is calculated by the NEGF method [26]. For the given charge density, the Poisson's equation is solved in order to obtain electrostatic potential in the nanotube channel. Then, the calculated potential profile is used as an input for NEGF equation, and an improved estimate is obtained for the charge density. This procedure is repeated until the convergence is achieved. At this time, all the physical quantities are accurate and current can be calculated.

The important calculation part in the NEGF simulation is finding the retarded Green's function, with regard to equation (1). The Hamiltonian matrix calculation for the carbon nanotube channel using the real space, and considering only one orbital for each atom is resulted in a matrix, the dimensions of which are equal to total number of carbon atoms. In the CNTFETs, the mode space approach is an appropriate method for the Hamiltonian calculation of the channel, since this method significantly reduces the Hamiltonian matrix dimensions.

The proposed device specifications are simulated through self-consistent solution of the Poisson and the Schrödinger equations and using the non-equilibrium Green's function by considering the mode space approach. In addition, only the orbitals are considered and tight binding approximation is used.

RESULTS AND DISCUSSION

In order to evaluate the electrical characteristics of the proposed structure, the current voltage (I_{DS}-V_{GS}) characteristics of the proposed structure are compared with the conventional structure as shown in Fig. 3. Fig. 3 is plotted for a drain-source voltage of 0.3 V (e. g V_{DS}= 0.3 V). As can be seen from the figure, am-bipolar behavior and OFF current are improved in the proposed structure, while the ON specifications such as sub-threshold swing and saturation current have not changed significantly.

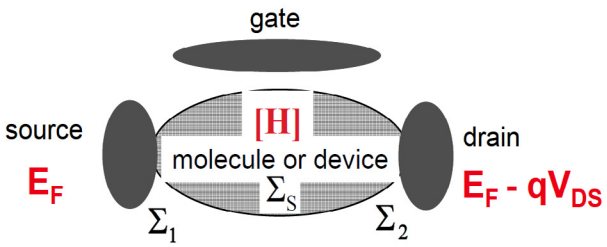

Fig. 2: Representation of quantities in the NEGF calculation [26].

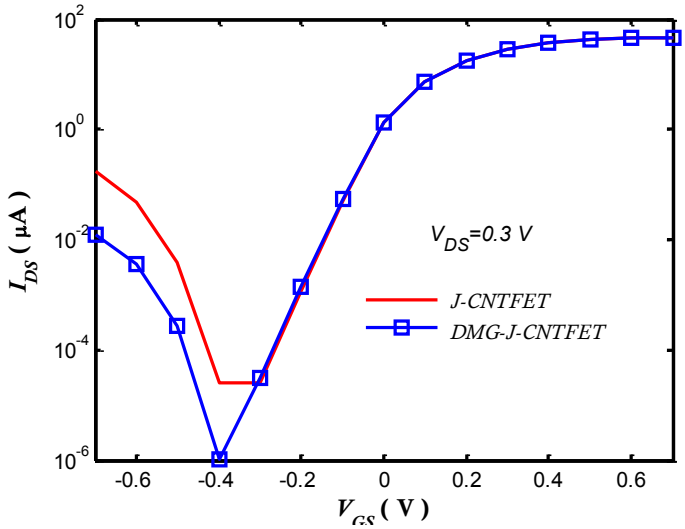

Fig. 3: Comparison of I_{DS}-V_{GS} characteristics of the DMG- J-CNTFET (symbol) with the conventional J-CNTFET at V_{DS}=0.3 V.

This improvement makes the proposed structure suitable to use as a CMOS transistor. For better justification of this behavior, Fig. 4 shows the number of electrons per unit energy along the channel for both devices, once in the ON state (e. g V_{DS}=0.3 V, V_{GS}=0.6 V), and once again in the OFF state (e. g V_{DS}=0.3 V, V_{GS}= -0.4 V). As can be seen, in the ON state (Fig. 4 (a) and (b)), by increasing the gate voltage, the potential barrier is reduced in the channel region and carriers are passing over the channel and reaching the drain, and there are no obstacles in the current passing through the channel region, therefore, both structures will have almost the same ON current. However, in the OFF state, in the proposed structure under the right gate (G_2), near the drain, a step potential is created in the energy band structure which increases the width of tunneling area and reduces the am-bipolar and OFF current.

Afterwards, in Fig. 5, I_{DS}-V_{DS} characteristics of both structures are illustrated for different gate source voltages of V_{GS}=0.3 V, 0.5 V. As explained and anticipated earlier, both structures have the same behavior in the linear and the saturation regions. Thus, increasing the gate voltage has increased the ON current in both devices.

For closer examination of device performance, the I_{ON}/I_{OFF} current ratio versus I_{ON} at V_{DS}=0.3 V is shown in Fig. 6. For plotting this figure, methods of [27, 28] are used. Considering a window with 0.3 V width in I_{DS}-V_{GS} curve, I_{ON} and I_{OFF} values for V_{GS} and V_{GS}(ON)-0.3 V would be achieved, respectively and thus, the curves are drawn by moving this window with 0.02 V steps.

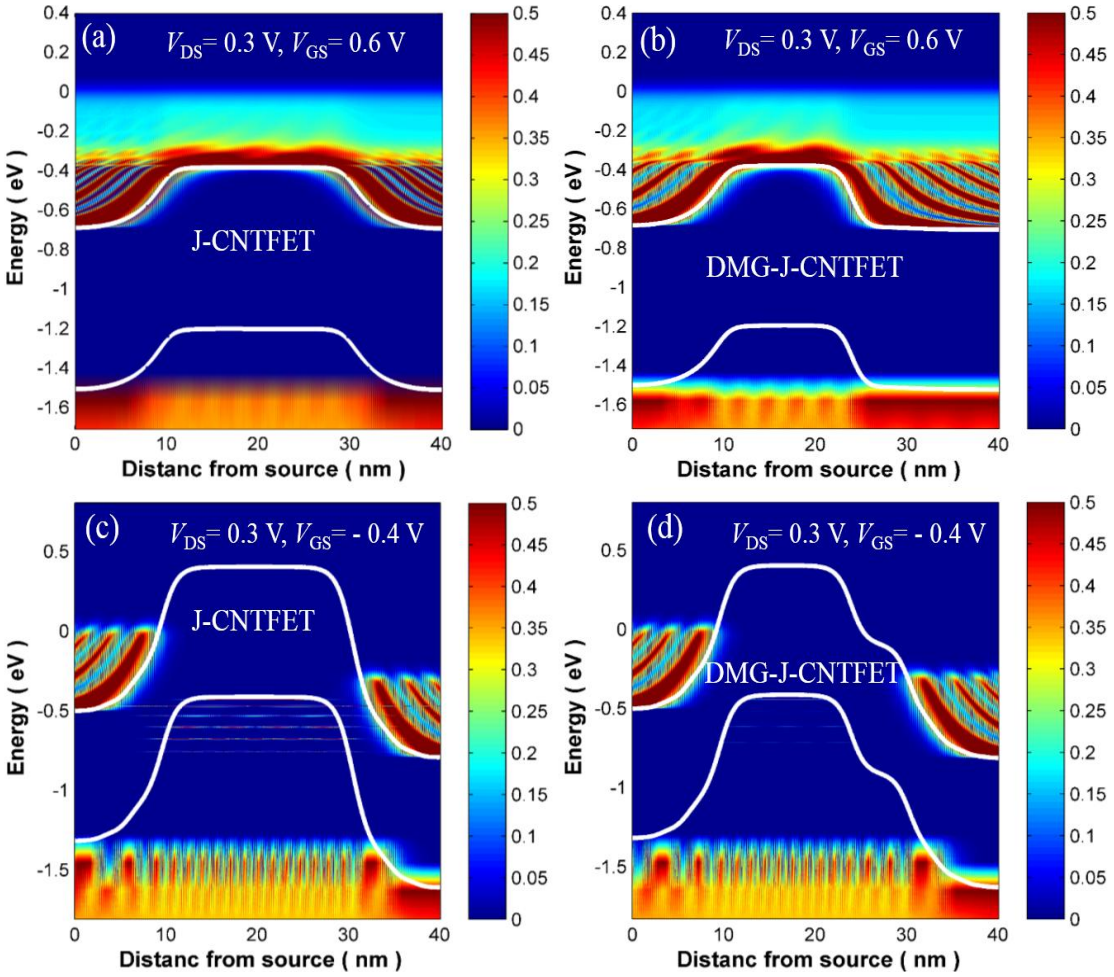

Fig. 4: Comparison of the energy band diagrams (white lines) and the electron density spectrum across the conventional J-CNTFET biased at V_{DS}=0.3 V and (a) V_{GS}=0.6 V (c) V_{GS}=-0.4 V and the proposed DMG-J-CNTFET biased at V_{DS}=0.3 V and (b) V_{GS}=0.6 V and (d) V_{GS}=-0.4 V.

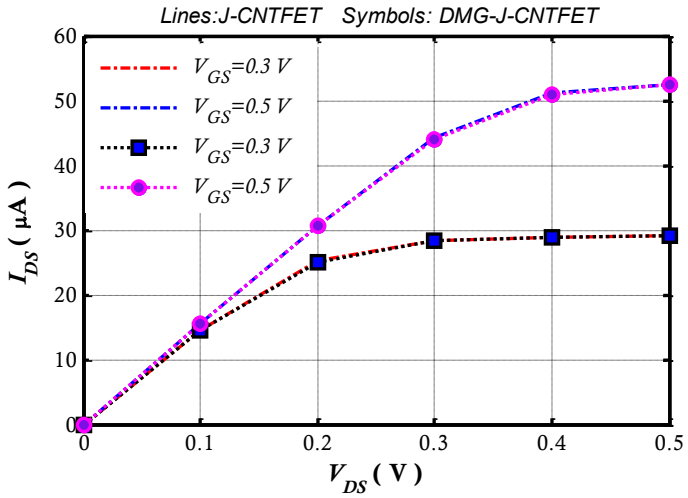

Fig. 5: I_{DS}-V_{DS} characteristics of DMG-J-CNTFET (symbols) compared with those of conventional J-CNTFET (lines) for various V_{GS}.

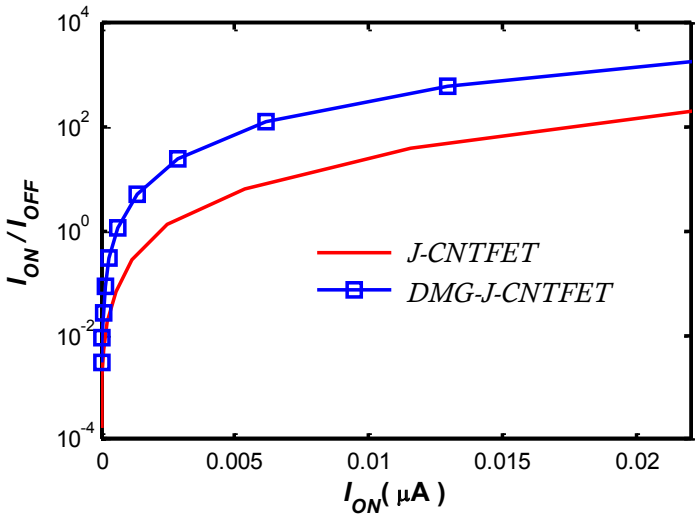

Fig. 6: ON/OFF current ratio versus ON-current at V_{DS}=0.4 V for the conventional J-CNTFET (line) and DMG-J-CNTFET (symbol).

As can be seen in the figure, the proposed structure, due to less OFF current, has higher I_{ON}/I_{OFF} current ratio. The inherent delay (τ) and power delay product (PDP) are two determining parameters in the switching behavior of the devices, which are calculated using the following equations [1].

$$\tau=\frac{Q_{ON}-Q_{OFF}}{I_{ON}} \quad (5)$$

$$PDP=(Q_{ON}-Q_{OFF})\times V_{DD} \quad (6)$$

In the above equation, Q_{ON} and Q_{OFF} show the total source-drain charges of the device in ON and OFF states, respectively. Fig. 7 (a) and (b) represent the comparison of inherent delay and PDP for both transistors, respectively.

As can be seen, the proposed structure has higher PDP and delay than the conventional structure. In order to justify this behavior, the number of electrons per unit energy along the device for both structures is shown in Fig. 8 (a) and (b), respectively. Since there is charge carrier accumulation in the new structure under the right gate (G_2), ΔQ (Q_{ON} - Q_{OFF}) is increased. As a result, more time is required to discharge these additional charges from this region, which will lead to further delay. For more comparison, the changes of electric field along the device for the

aforementioned structures are depicted in Fig. 9.

According to this figure, for the new structure, a peak for the electric field can be seen in conjunction of two gates. The reason is the step potential created in the energy band structure, which causes a sudden change in the energy band structure in this section. The presence of the field peak in the channel region increases the lifetime of the device as well as the greater gate control on the channel conductivity [9]. It can also be observed that the electric field close to the end of drain is reduced for dual material structure. The electric field peak near the end of drain makes the electrons enter the channel with low initial speed and gradually increase their speed toward the drain. Thus, the electron velocity near the drain is maximized, causing the hot carrier effect [10]. As a result, the proposed structure is also superior to the conventional structure in terms of hot carrier effect. The average velocity along the devices is shown in Fig. 10, which is consistent with the descriptions in the previous section.

As explained earlier, the optimal choice for the work-function difference between the two metal gates is 0.5 eV, length of left gate (G_1) near the source area is 14 nm, and length of right gate (G_2) adjacent to the drain is 6 nm. So far, all the comparisons are made with this assumption, ensuring that the above selection had been an optimal choice.

Fig. 11 shows the I_{DS}-V_{GS} characteristic of the new device with various work-function differences (e. g φ_{M2} - φ_{M1}= -0.3, -0.5, -0.8). As mentioned above, the second gate (G_2) has a lower work-function than the first gate (G_1).

In Fig. 12, the gate length of 20 nm is remained

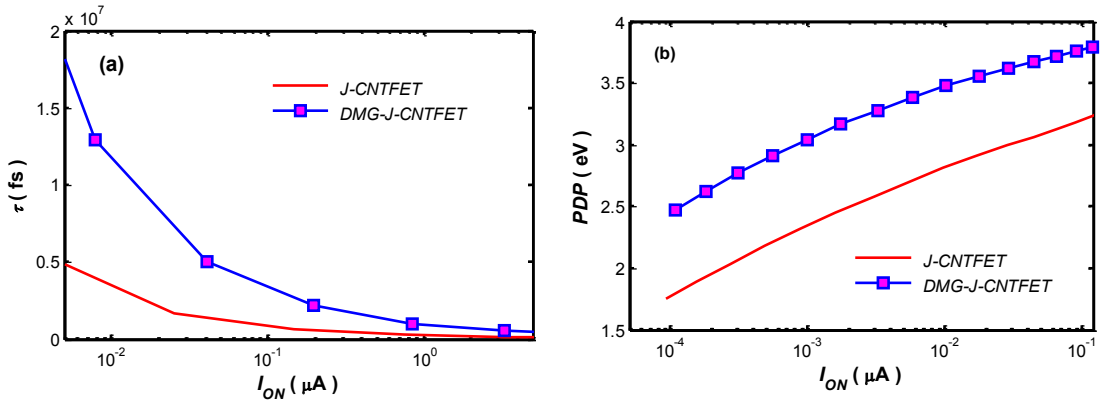

Fig. 7: Comparison of (a) delay time and (b) PDP versus ON-current of the conventional J-CNTFET (line) and DMG-J-CNTFET (symbol).

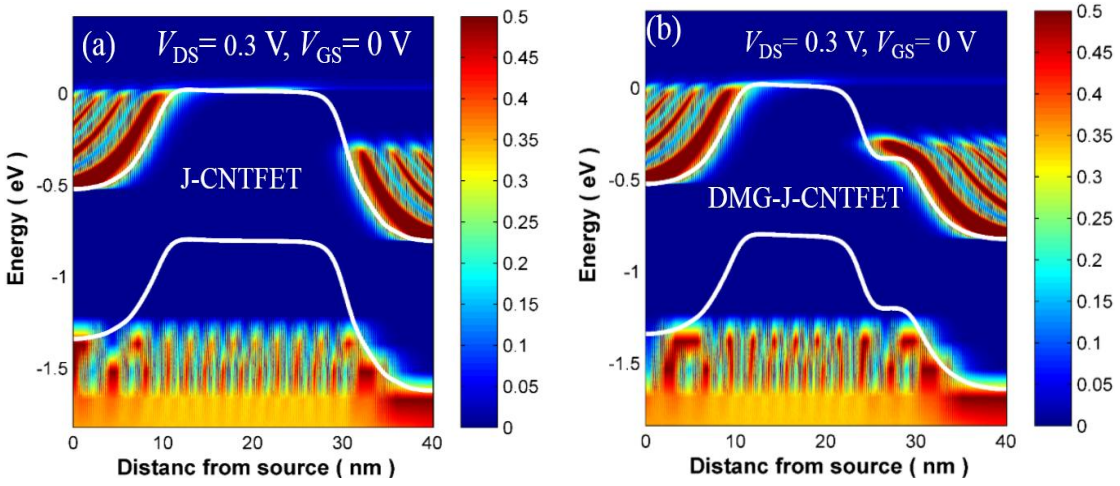

Fig. 8: Energy band diagrams (white lines) and the local density of states across the (a) conventional J-CNTFET and (b) DMG-J-CNTFET both biased at V_{DS}=0.3 V and V_{GS}=0 V.

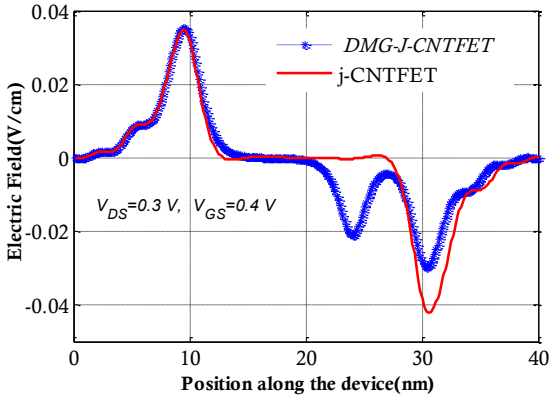

Fig. 9: Electric field profile along the device for the conventional J-CNTFET (line) and DMG-J-CNTFET (symbol) at V_{DS}= 0.3 V and V_{GS}=0.4V.

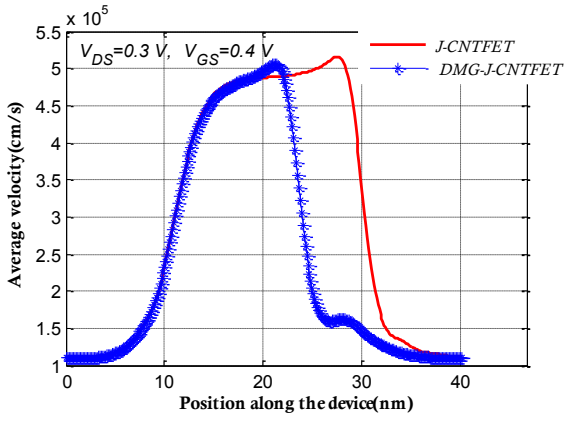

Fig. 10: Average velocities of the carriers along the device for the conventional J-CNTFET (line) and DMG-J-CNTFET (symbol) at V_{DS}= 0.3 V and V_{GS}=0.4V.

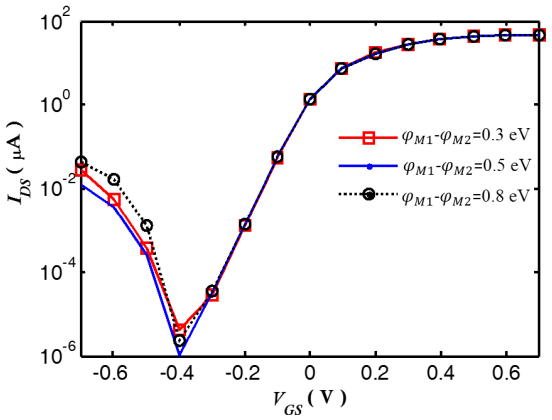

Fig. 11: The variation in I_{DS}-V_{GS} characteristics of the proposed structure by change in gate work function difference.

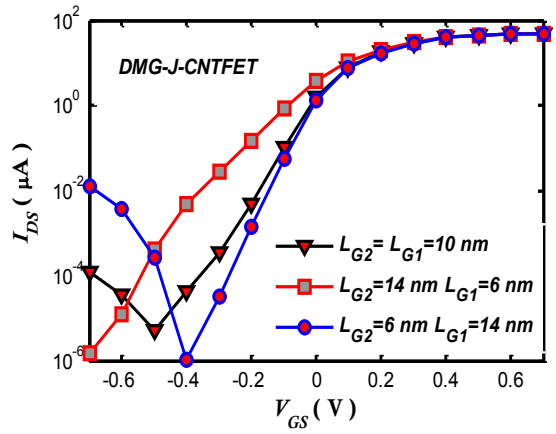

Fig. 12: The variation in I_{DS}-V_{GS} characteristics of the proposed structure by change in second gate length.

constant (L_{G1}+L_{G2}=20 nm), and I_{DS}-V_{GS} characteristic is examined by changing the length of the second gate (L_{G1}=L_{G2}=10 nm, L_{G2}=14 nm and L_{G1}=6 nm, L_{G2}=6 nm $L_{G1=}$14 nm).

As can be seen in Figs. 11 and 12, the lowest leakage current and sub-threshold swing are in work-function difference of 0.5 eV (φ_{M2}- φ_{M1}=-0.5) and gate length of L_{G2}=6 nm and L_{G1} =14 nm.

CONCLUSION

In this article, in order to simulate the electrical characteristics of the proposed structure named dual material gate junctionless carbon nanotube field effect transistor (DMG-J-CNTFET), the non-equilibrium Green's function method (NEGF) is used in the mode space approach. The simulation results show that the proposed structure in comparison with the conventional one has better am-bipolar behavior and lower OFF current, I_{ON}/I_{OFF} current ratio is improved and ON state characteristics of the device such as sub-threshold swing and ON current are not degraded. Furthermore, the hot carrier effects are also reduced in the new structure.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this manuscript.

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