

Analysis and study of geometrical variability on the performance of junctionless tunneling field effect transistors: Advantage or deficiency?

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Abstract

This study investigates geometrical variability on the sensitivity of the junctionless tunneling field effect transistor (JLTFET) and Heterostructure JLTFET (HJLTFET) performance. We consider the transistor gate dielectric thickness as one of the main variation sources. The impacts of variations on the analog and digital performance of the devices are calculated by using computer aided design (CAD) tools. The gate oxide thickness is varied uniformly from right to left and vice versa and the performance of devices are analyzed. It is shown that changes in the geometric dimensions of the devices improves some electrical parameters and degrades others. Finally, we use the oxide thickness variation advantage and implement the oxide pocket close to the drain-channel interface for proposing of the pocket in narrower drain side oxide HJLTFET (PNS-HJLTFET).

Keywords: Ambipolar Current; Geometrical Variability; Heterostructure; Junctionless Tunnel Field-effect transistor; Oxide pocket

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INTRODUCTION

Tunneling Field Effect Transistors (TFETs) have attracted widespread attention in recent years due to low Sub-threshold Slope (SS) and low power consumption. TFETs are also immune to short channel effects (SCEs) because the current mechanism in the TFETs is controlled by the band to band tunneling [1-5]. SS in conventional MOSFETs is limited to values greater than 60 mV/Dec ($2.3kT/q$), which does not provide high ratios for low power applications (I_{on}/I_{off}). The low ON-state current in silicon TFETs is a major challenge due to poor BTBT rate. In order to improve on current methods such as strain engineering, hetero-structures, low band-gap materials, high-K insulators and nanowires have been employed [6-9]. In contrast, low SS in TFETs can reduce the threshold voltage and device power to values less than 0.5 V. In the term of scaling, random variations

in performance of TFETs due to Random Dopant Fluctuation (RDF) may be significant. RDF effects have been reported as unacceptable increases in the OFF-state current [10-11].

The other issue about TFETs is the ambipolar behavior that limits the design of digital circuits. In negative gate biases, an overlap is made between the channel valence band and the drain conduction band. As a result, the electrons tunnels from the channel to drain. In this way, TFETs exhibit a significant current at both the positive and negative biases. To suppress this parasitic behavior, methods such as using Gaussian doping profiles, gate/drain overlap, hetero-structure insulators and gate work function engineering [12-15]. One of the main challenges in experimental realization of steep transistors is the sensitivity of device performance to design parameters. Ideally, the steep transistor should have a high

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sensitivity to only the gate voltage in the sub threshold region; however, it is shown here that the conventional TFETs have an increased sensitivity to device parameters like the oxide thicknesses. High sensitivity to variability in device parameters reduces the reliability of integrated circuits made from these devices. This issue has been thoroughly investigated in MOSFETs and the main sources of fluctuations including Random Discrete Dopant (RDF), Line Edge Roughness (LER), Poly-silicon granularity and variations in oxide thickness have been studied extensively[16-18]. The same requirements for TFETs are also in place.

All MOSFETs are based on the use of junctions between semiconductors. Because of the laws of diffusion and the statistical nature of the dopant atoms in the semiconductor, the fabricating and formation of ultra-shallow and abrupt junctions with high doping concentration gradients has become an increasingly expensive and difficult. Impurities in such fabrication diffuse from the source/drain to the channel. This problem can be solved with junctionless TFETs (JLTFETs), which have exhibited promising performance for analog and digital applications [19- 21]. From the literature review, it is evident using heterostructure material at source/channel interface is a possible way of improving the performance of TFETs especially ON state current [22-27].

This study investigates the effect of uncertainties in device geometry parameters on its

performance. The precise design of the geometric dimensions of the device has a significant impact on its performance. The accuracy of design depends on the technology used. However, some uncertainties in the geometric dimension of the device are inevitable. Of course, the tolerance level is determined by the International Technology Roadmap for Semiconductor (ITRS). This study considers the uncertainties in gate dielectric thickness. The rest of the paper is organized as follows:

Device structure and simulation method/models will be presented in section 2. In sections 3, DC characteristics of devices and Strategy of studying the parameters variations will be discussed. Also In section 3 performance of studied devices will be analyzed and a structure will be proposed. Finally conclusion of this report will be presented in section 4.

EXPERIMENTAL

Device structures and simulations

A 2D-structure of junction less tunneling field effect transistor (JLTFET) is illustrated in Fig. 1. Physical characteristics of devices are given in Table 1. Drain, Source and channel regions are uniformly doped with donor dopant at concentrations of $1 \times 10^{19} \text{ cm}^{-3}$. The SiO_2 insulator with a thickness of 2 nm separates the control gate(c-gate) and polarity gate (p-gate) from channel and source. Heterostructure junctionless tunneling field effect

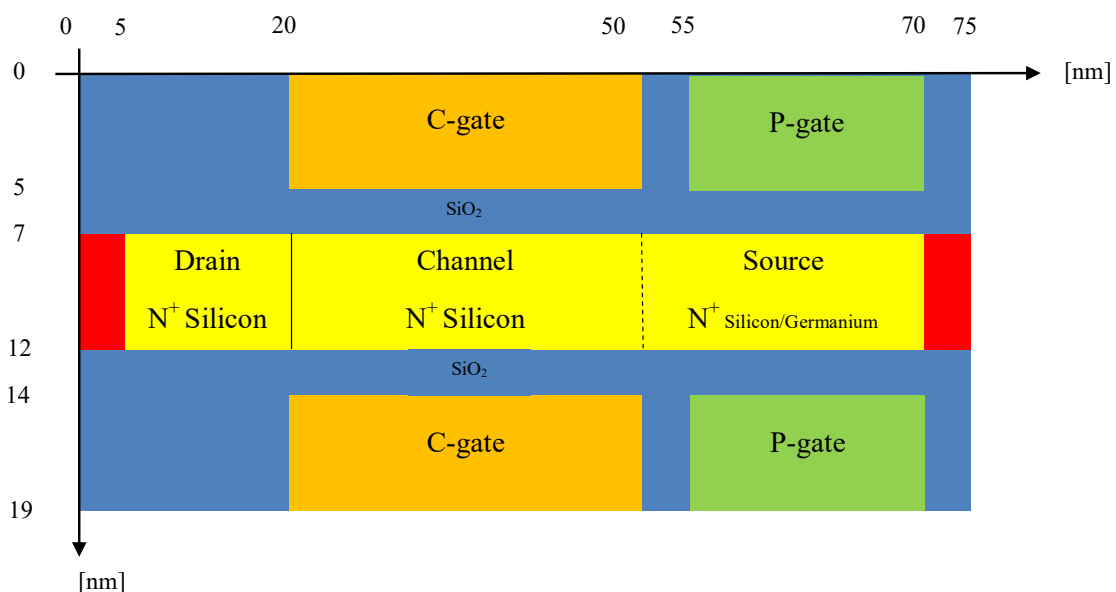


Fig. 1: Schematic view of JLTFET/HJLTFET.

transistor (HJLTFET) is formed when the source region is replaced with Germanium. The silicon/germanium body thickness is 5 nm.

SILVACO ATLAS 2D 5.19.20 R is employed for all simulations which uses nonlocal Band to Band Tunneling (BTBT) model to compute tunneling probability at tunneling junction. The tunneling current in the nonlocal BTBT at each point is independent of the electric field and dependent on band structure variation along the device. Because of high-impurity atoms in the channel and due to interface trap effect, the Shockley Read Hall (SRH) and Auger (AUGER) recombination models were included in the simulation. We incorporated the effect of Fermi-Dirac statistics in the calculation of the intrinsic carrier concentration required in the expressions for SRH recombination. Assuming high doping concentration, a band-gap narrowing model (BGN) was also included. Quantum confinement effects on BTBT were induced through the use of the quantum confinement model given by Hansch (HANSCHQM). To include a mobility model into the simulation, the Lombardi mobility model (CVT) also employed. Given the important role of trap-assisted tunneling (TAT) in the sub threshold region, the TAT model given by Schenk (SCHENK.TUN) is enabled. The nonlocal BTBT used in this study calculates electron/hole tunneling probability on the basis of equation (1) which is known as Wetzell-Kramer-Brillouin (WKB) approximation method [28-30].

$$T_t \approx \exp\left(-\frac{4}{3} \frac{\sqrt{2m^*}}{q\hbar(E_g + \Delta\phi)} (E_g)^{3/2}\right) \quad (1)$$

where m^* is the electron effective mass, q is the electron charge, \hbar is the reduced Plank constant, $()$ is the screening tunneling length of the barrier that depends on device geometry, E_g denotes the energy band gap, and $\Delta\phi$ represents the energetic difference between the valence and conduction bands of tunneling regions. Drain current depends on tunneling probability, which itself is dependent on band structure variation at the interfaces of the channel with source/drain.

RESULTS AND DISCUSSION

DC Characteristics

Applying gate and drain voltages, the band bending in energy band structure will be occurred and tunneling probability rises at regions where the conduction band overlaps with the valence band. In JLTFETs, BTBT may occur in two different manners. The first is the on-state, during which

positive gate voltage is applied and an overlap occurs between the conduction band of the channel and the valence band of the source. The second is the ambipolar state, at which negative gate voltage is applied and an overlap occurs between the conduction band of the drain and the valence band of a channel.

In order to calibrate the model, it is necessary to compare the simulation results with the reference data [31]. For this, the parameters used in models, especially nonlocal BTBT, should be modified in order to match the simulation results with reference data. Fig. 2 shows this calibration. A good agreement between simulation and reference results is observed.

The energy band diagram of JLTFET and H-JLTFET in ON and OFF state are shown in Fig. 3(a) and Fig. 3(b) respectively. As we expect, tunneling barrier or tunneling length in ON state decreased at source side in both JLTFET and HJLTFET. It is clear that in the ON state, tunneling length is narrower and electrons can tunnel from valence band of source to conduction band of the channel and the tunneling rate and consequently drain current will be increased. The tunneling barrier reduction in HJLTFET is more due to lower energy band gap of germanium.

The intrinsic gate capacitance is an important parameter for the RF performance analysis especially in calculating cut-off frequency[31-35] we investigate the analog performance of n-type double gate junctionless tunnel field effect transistor (DG-JLTFET). The intrinsic gate capacitance is extracted from small signal AC simulation at frequency of 1 MHz. The total gate capacitance consists of gate to channel capacitance plus gate to source/drain capacitance. The variation of total gate capacitance (C_{gg}) along with C_{gd} and C_{gs} respect to gate voltage are plotted in Fig. 4(a) and Fig. 4(b). It is observed From Fig. 4, that the value of gate capacitance for the HJLTFET is higher than that of the JLTFET for all values of gate voltages. In the HJLTFET, because of lower energy band gap at source side, more carriers can tunnel from the source valence band to the conduction band of the channel. Therefore the population of carriers and consequently the gate capacitance for HJLTFET is more than JLTFET. As the gate voltage increases, the length of the tunneling barrier decreases, which also reduces the C_{gs} . It is worth noting that in both structures the C_{gs} is negligible and C_{gd} is dominant in total gate capacitance. Given that the

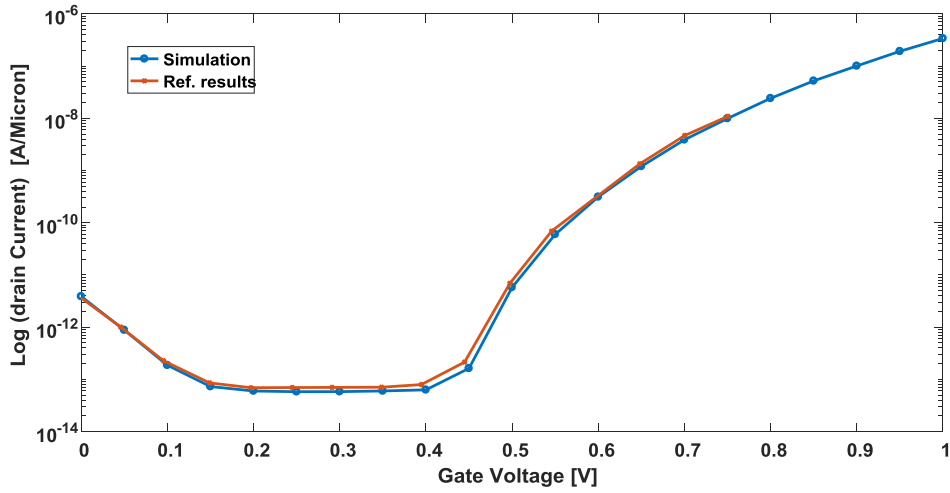


Fig. 2: Simulation calibration against data from Ref. [27].

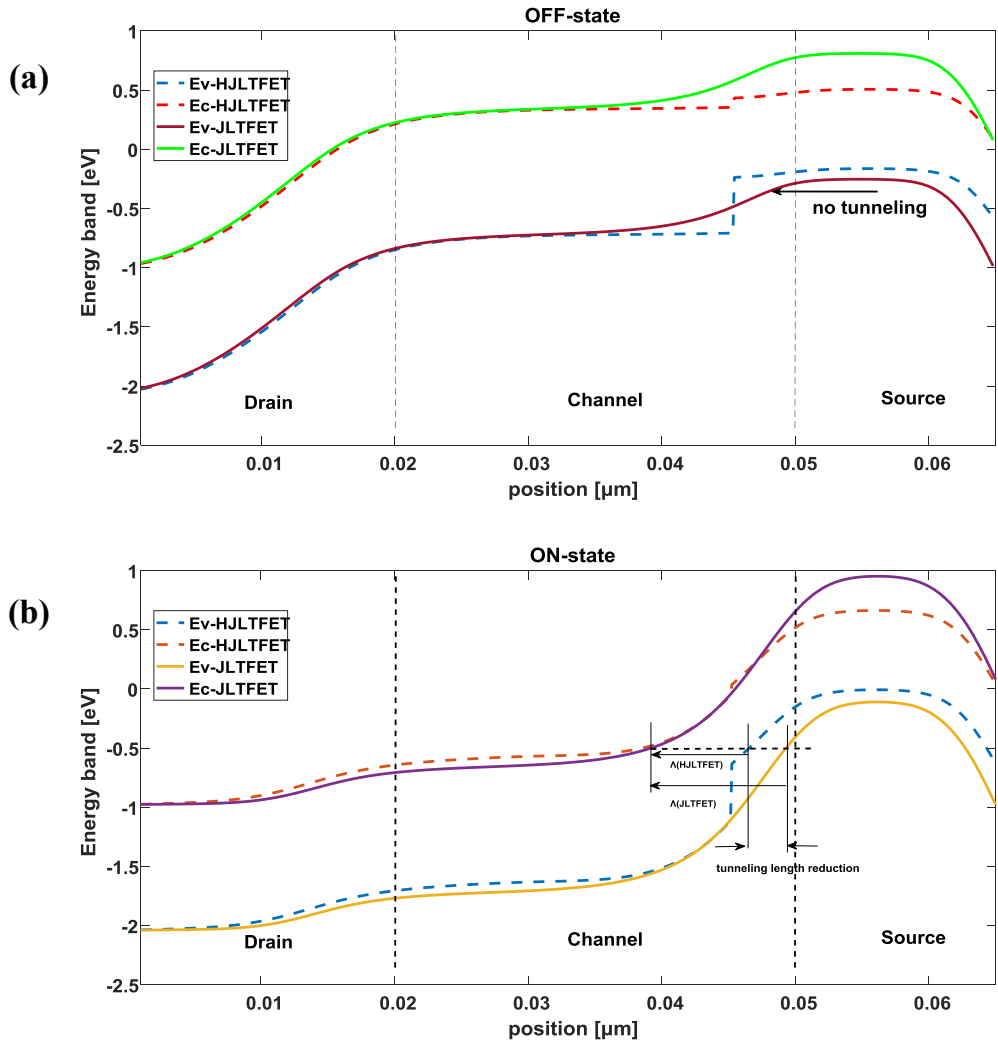


Fig. 3: Energy band diagram of JLTFT/HJLTFT: a) OFF state b) ON state.

drain-channel tunneling junction is still inactive at the positive gate voltages, the C_{gd} increases. This means that the tunneling resistance at drain side increases.

The drain current for two structure is shown in Fig. 5. A more accurate comparison between some important parameters of JLTFET and HJLTFET is shown in Table 2. It can be seen that, except for ambipolar current, other parameters have been improved.

Strategy of studying the geometrical parameters variations

The current study only includes uncertainty in the gate oxide thickness. The effect of uncertainty on the characteristics of the transistor will be discussed. Two approaches are considered as follows:

a-The thickness of the gate oxide decreases uniformly with constant slope from right to left. We refer to this as JLTFET/HJLTFET with Narrower

Table 1: Device design and material parameters.

Parameter name	Symbol	Value	unit
Gate oxide thickness	t_{ox}	2	nm
Silicon body thickness	t_{si}	5	nm
Drain/Channel/Source doping concentration	N_D	1×10^{19}	cm^{-3}
C-gate work function	W_C	4.7	eV
P-gate work function	W_{DP}	5.93	eV
Dielectric constant	K	3.9	-

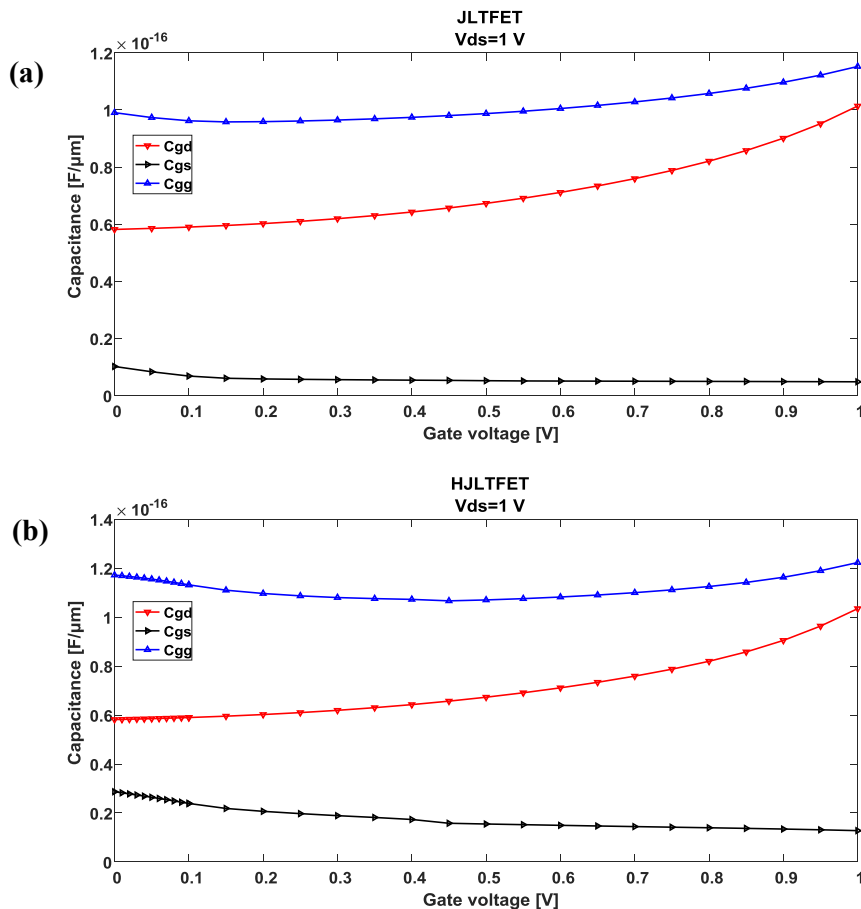


Fig. 4: Capacitance in On-state for: a) JLTFET b) HJLTFET [$V_{ds}=1V$ and $V_{gs}=1V$].



Drain side oxide or briefly ND-JLTFET/ND HJLTFET.

b-The thickness of the gate oxide decreases uniformly with constant slope from the left to right. We refer to this as JLTFET/ HJLTFET with Narrower Source side oxide or briefly NS-JLTFET/ NS-HJLTFET.

In both cases, it is assumed that the variation is at most 10% of nominal value. In all simulation steps both two approaches are compared with the base mode which has uniform gate oxide thickness. The aforementioned scenarios are shown in Fig. 6(a) and Fig. 6(b) respectively.

The output characteristic curve of JLTFET/ HJLTFET in two aforementioned scenarios along with the base mode is shown in Fig. 7. The HJLTFET demonstrates more ON current for all scenarios in comparison with JLTFET. However only NS-HJLTFET shows improvement in ON current with 8% and other cases cannot improve ON current. Due to no change in drain material, ambipolar current has no significant change.

Based on equation (1), the tunneling length (Λ) depends on the characteristics of the semiconductor material and device geometry and insulator characteristics [36]. The variation arisen from oxide thickness, causes band bending in energy band diagram. As a result the tunneling length and the tunneling rate/current will be changed. In according to simulations results, although the variation in the energy band diagram seems to be negligible, but due to the exponential dependence of the drain current to band bending, changes in tunneling rate and drain current will

be significant. Since the tunneling phenomenon is the direct result of changing in the energy band diagram, it seems reasonable to focus analysis on any changes in the shape of this diagram. Based on equation (1), the tunneling length (Λ) depends on the characteristics of the semiconductor material and device geometry and insulator characteristics [28]. The uncertainties caused by the insulating thickness, induces a change in the shape of the energy band diagram. As a result the tunneling length and consequently the tunneling rate/current are changed. In according to simulations results, although the variation in the energy band diagram seems to be negligible, but due to the exponential dependence of the drain current to band bending, changes in tunneling rate and drain current will be significant.

Performance assessment

Some important parameters used in performance assessment are shown in Table 3. A comparative data for aforementioned scenarios and parameters is shown in Fig. 8. The relative change for any parameter shown in Fig. 8 is derived from equation (2), (e.g. for SS):

$$\frac{SS_{ND-JLTFET} - SS_{JLTFET}}{SS_{JLTFET}} \times 100 \tag{2}$$

The off current and I_{ON}/I_{OFF} ratio especially in the ND-JLTFET/HJLTFET are more sensitive to variation. For NS-HJLTFET the only parameter which shows severe changes is ambipolar current and the other have no change or even have been improved(e.g. threshold voltage and I_{ON} and also I_{ON} to I_{OFF} ratio).

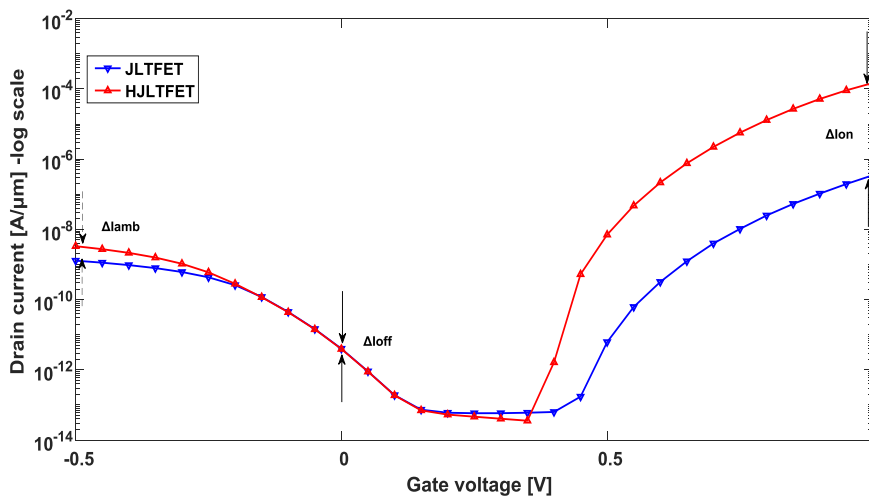


Fig. 5: Drain current for JLTFET and HJLTFET [$V_{ds}=1V$ and $V_{gs}=1V$].



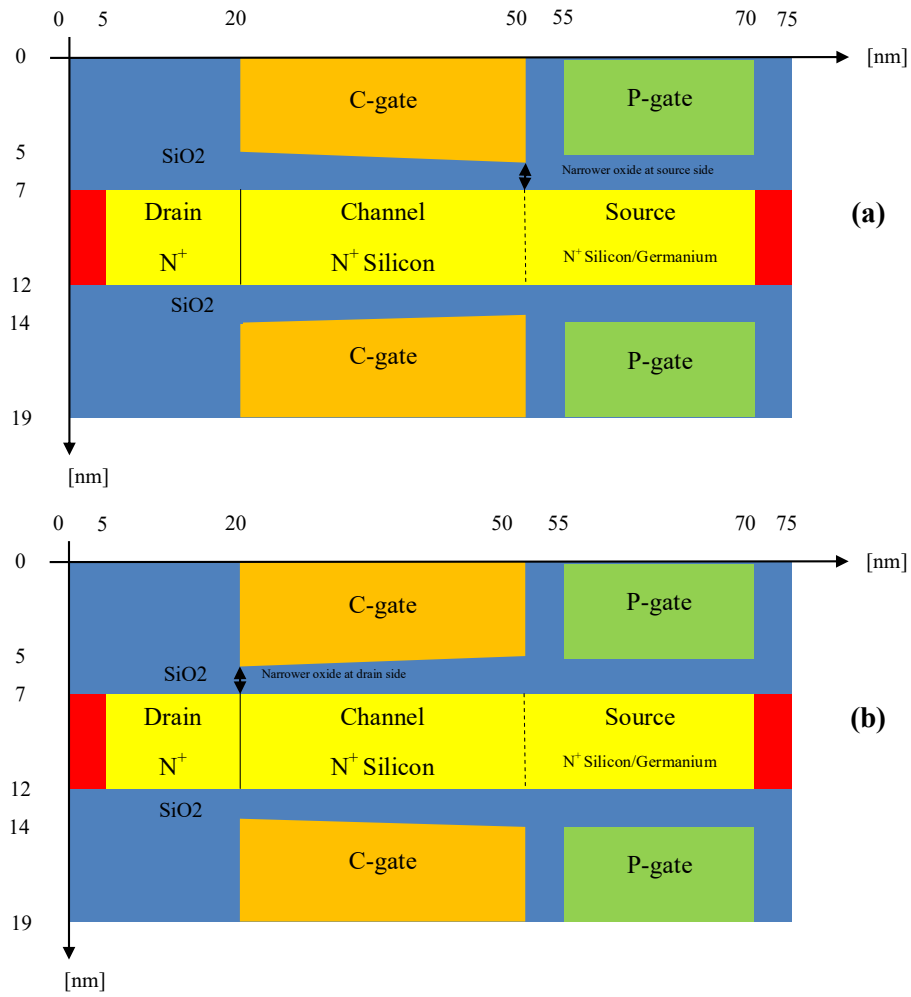


Fig. 6: Uniform change in gate oxide thickness a) NS-JLTFET/NS-HJLTFE b) ND-JLTFET/ND-HJLTFE.

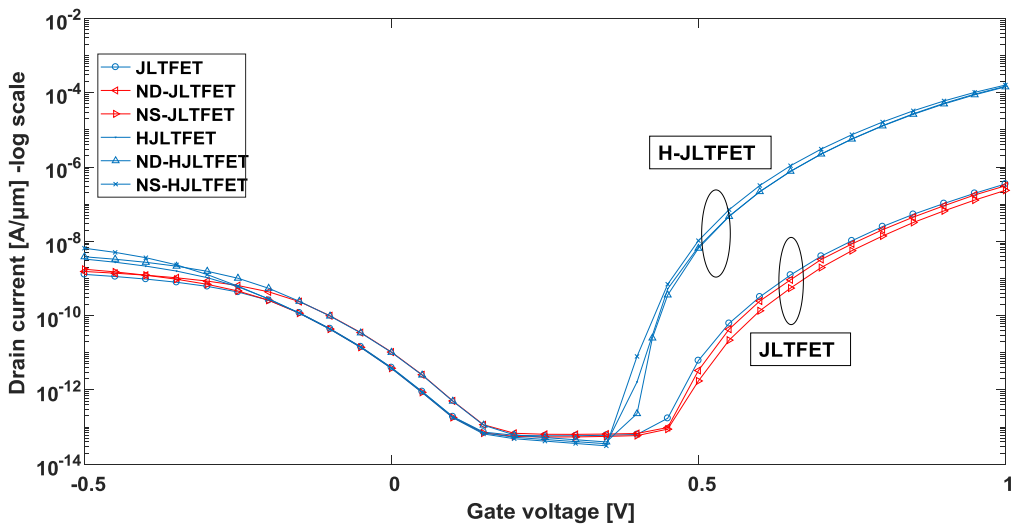


Fig. 7: Drain current for JLTFET and HJLTFET along with ND and NS modes [$V_{ds}=1V$ and $V_{gs}=1V$].

This implies that NS-HJLTFET can be considered as an advantage not challenge if ambipolar current be suppressed significantly.

Proposed structure

Static and dynamic power dissipation in inverter based logic circuits depend on V_{DD} and OFF state leakage current [37]. Although TFETs are considered as energy efficient devices, but to realize the application of TFETs into circuit level, the ambipolar behavior should be well controlled. Given that the ambipolar current occurs in drain-channel tunnel junction at negative gate bias due to overlap between valance band of channel and conduction band of drain, it is appropriate to reduce the tunneling rate in this junction. In according to Table 4, it seems reasonably to propose a method to compensate the drawback of NS-HJLTFET along

with keeping its advantages. If a small area of the gate oxide close to the drain-channel interface is grown thicker, the aforementioned target will be realized. We call this proposal as pocket oxide in NS-HJLTFET (PNS-HJLTFET). The proposed structure is shown in Fig. 9.

Fig. 10(a) shows the effect of the pocket oxide on the energy band diagram of NS-HJLTFET in the ambipolar state. It clearly shows that there is no significant change in tunneling barrier width. This narrowing of tunneling barrier leads to suppression of the ambipolar current.

Fig. 10(b) illustrates the drain current of NS-HJLTFET and PNS-HJLTFET. In order to investigate the effect of geometrical variability on the analog performance, the transconductance variations for all aforementioned cases are shown in the Fig. 10(c). It is seen that NS-HJLTFET has less variation

Table 3: Relative change of Performance for JLTFET and HJLTFET in various scenarios.

	JLTFET			HJLTFET		
	Base	ND	NS	Base	ND	NS
$SS \left[\frac{mV}{dec} \right]$	32.2	32.5	38.5	20	12.3	20.7
V_t [V]	0.38	0.38	0.39	0.37	0.37	0.36
$I_{ON} \left[\frac{A}{\mu m} \right]$	3.5×10^{-7}	3.11×10^{-7}	2.35×10^{-7}	1.48×10^{-4}	1.43×10^{-4}	1.6×10^{-4}
$I_{OFF} \left[\frac{A}{\mu m} \right]$	4.0×10^{-12}	1.04×10^{-11}	3.8×10^{-12}	3.92×10^{-12}	1.0×10^{-11}	3.8×10^{-12}
$\frac{I_{ON}}{I_{OFF}}$	8.75×10^4	3.0×10^4	6.18×10^4	3.77×10^7	1.43×10^7	4.2×10^7
$I_{AMB} \left[\frac{A}{\mu m} \right]$	1.28×10^{-9}	1.54×10^{-9}	1.77×10^{-9}	3.33×10^{-9}	3.83×10^{-9}	6.52×10^{-9}

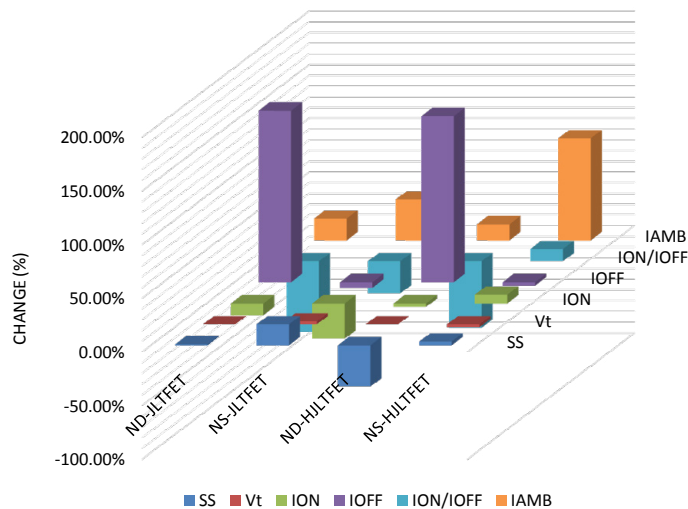


Fig. 8: Relative change of Performance for JLTFET and HJLTFET in various scenarios.

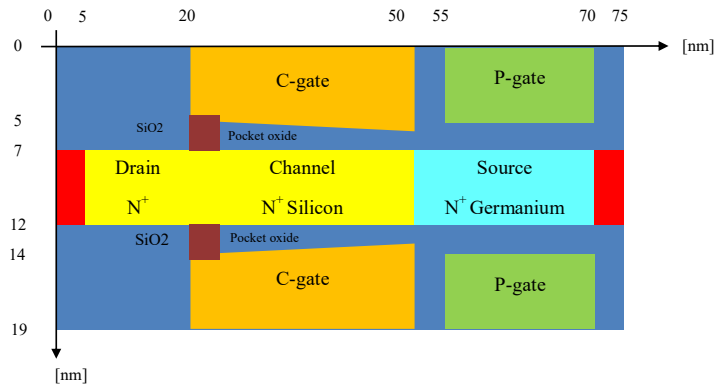


Fig. 9: The proposed structure for NS-HJLTFET.

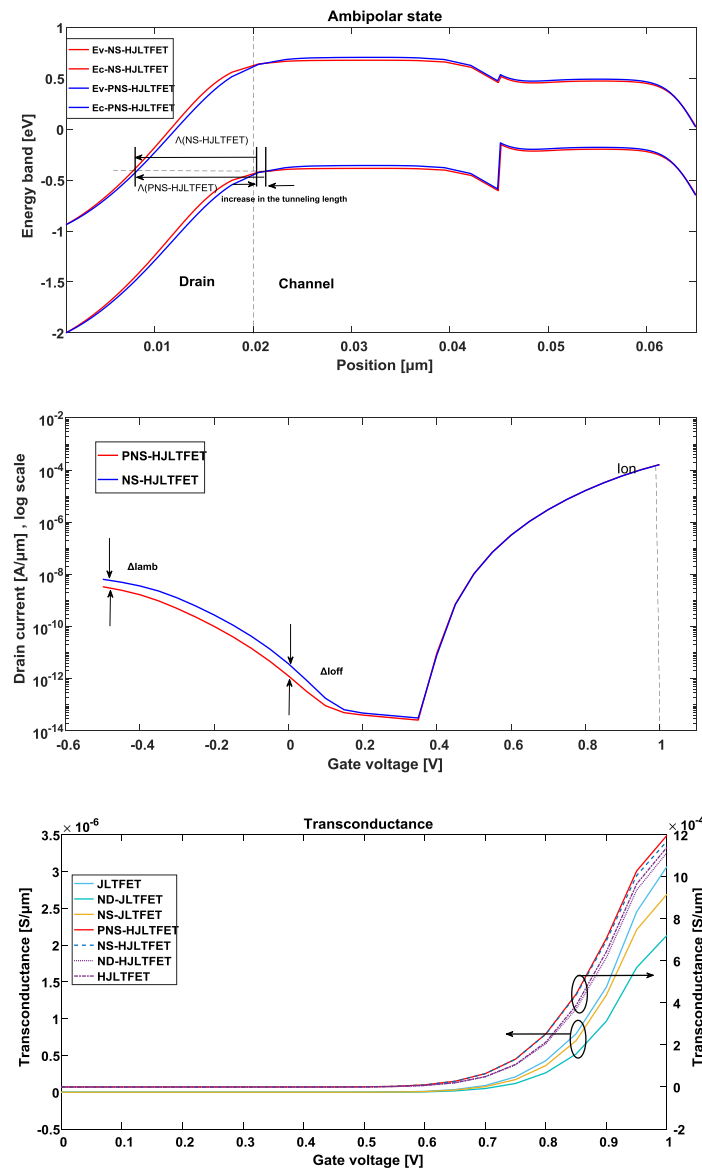


Fig. 10: Effect of pocket oxide on: a) Energy band diagram b) ambipolar current in ambipolar state [$V_{ds}=1V$ and $V_{gs} = -0.5 V$] c) Transconductance for NS-HJLTFET and PNS-HJLTFET [$V_{ds}=1V$ and $V_{gs}=1.0 V$].

and also PNS-HJLTFET has the largest value of transconductance. Some of the extracted data have been listed in Table 4. The sub-threshold swing (SS) and also threshold voltage (V_t) for all structures are similar. Improvement of ON current for PNS-HJLTFET is 10%. However, the best improvement is seen for OFF current and I_{ON}/I_{OFF} . For PNS-HJLTFET, the improvement for OFF current, I_{ON}/I_{OFF} is 66.8% and 231% respectively.

For the n-TFET, the ambipolar current is a current due to the narrowing of tunneling barrier width at the channel-drain junction for negative gate bias [37]. This narrowing is due to the accumulation of holes in the channel. As the concentration of the accumulated holes increases, the tunneling barrier width gets narrower leading to a higher ambipolar current. Based on our proposed device which uses pocket oxide at the drain side of the channel, the accumulation of holes decreases and consequently the ambipolar is suppressed. Reduction in the hole concentration at channel near drain is shown in Fig. 11.

One of the important performance metric that

corresponds to intrinsic limitations on switching speed and AC operation of a transistor is intrinsic device delay time (τ) [38]. In this study the switching speed is calculated as:

$$\tau = C_g \frac{V_d}{I_{ON}} \quad (3)$$

Where C_g is gate capacitance and drain voltage V_d is 1V and I_{ON} is on state current of the device. The intrinsic delay time for HJLTFET, NS-HJLTFET and PNS-HJLTFET is shown in Fig. 12. It seen from Fig. 12, the delay time for HJLTFET is more NS-HJLTFET and PNS-HJLTFET for all gate voltages. However by increasing gate voltage NS_HJLTFET and PNS-HJLTFET have the same performance. Power-delay product (PDP) is the switching energy required for ON-OFF transition of a transistor. It is a measure of the dynamic power dissipation. In this study PDP is calculated by [38]:

$$PDP = C_g \times V_d^2 \quad (4)$$

Power-delay product (PDP) for HJLTFET, NS-HJLTFET and PNS-HJLTFET is shown in Fig. 13. At the low gate voltage the PNS-HJLTFET consumes

Table 4: Device performance for HJLTFET, NS-HJLTFET and PNS_HJLTFET.

	HJLTFET	NS-HJLTFET	PNS-HJLTFET
SS [$\frac{mV}{dec}$]	20	20	19.4
V_t [V]	0.37	0.36	0.36
I_{ON} [$\frac{A}{\mu m}$]	1.48×10^{-4}	1.6×10^{-4}	1.63×10^{-4}
I_{OFF} [$\frac{A}{\mu m}$]	3.92×10^{-12}	3.8×10^{-12}	1.3×10^{-12}
$\frac{I_{ON}}{I_{OFF}}$	3.77×10^7	4.2×10^7	1.25×10^8
I_{AMB} [$\frac{A}{\mu m}$]	3.33×10^{-9}	6.5×10^{-9}	3.3×10^{-9}

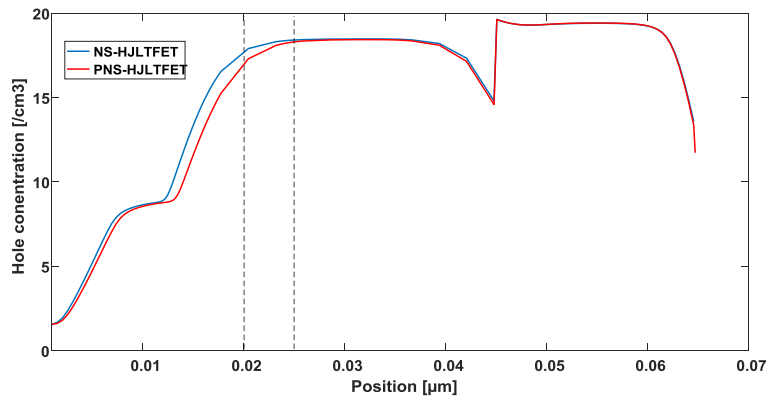


Fig. 11: Hole concentration in ambipolar state for NS-HJLTFET and PNS-HJLTFET [$V_{ds}=1V$ and $V_{gs}=-0.5V$].

the least energy for switching, however at higher gate voltages, the PNS-HJLTFET shows the moderate consuming energy in comparison with HJLTFET and NS-HJLTFET.

The output conductance(g_d) and the output resistance (R_o) of studied devices is calculated by [38]:

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \quad (5)$$

$$R_o = \left(\frac{\partial I_d}{\partial V_{ds}}\right)^{-1} \quad (6)$$

The variation of output conductance and resistance with respect to the variation in drain voltage is also shown in Fig. 14. From Fig. 14, we observe that the PNS-HJLTFET has a lower value of output resistance compared to the HJLTFET and

NS-HJLTFET, since the output conductance of the PNS-HJLTFET is higher than that of the two others for all values of drain voltages, as observed from the same Figure.

The unity gain frequency is shown in Fig. 15. The PNS-HJLTFET shows more cut-off frequency than HJLTFET. However f_T for NS-HJLTFET and PNS-HJLTFET has no meaningful difference. The f_T is calculated by [39], we present a detailed performance comparison between conventional n-i-n MOSFET transistors and tunneling field-effect transistors (TFETs):

$$f_T = \frac{g_m}{2\pi C_g} \quad (6)$$

Where g_m is transconductance and C_g is the gate capacitance of the device.

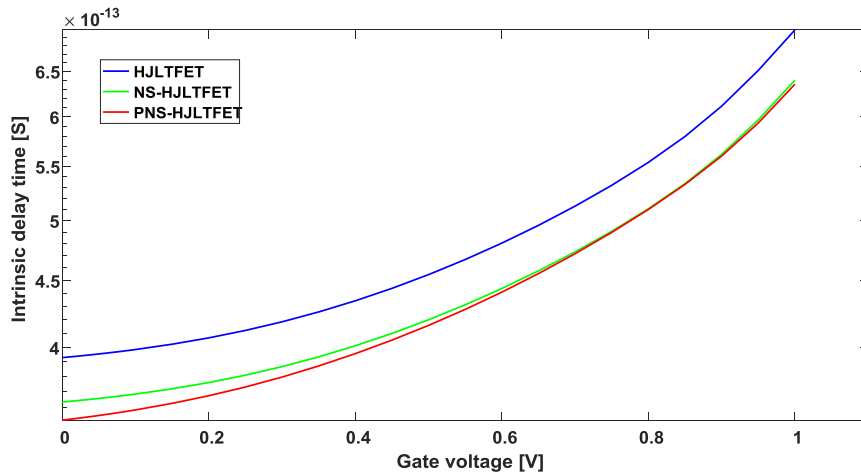


Fig. 12: Intrinsic delay time (τ) for HJLTFET, NS-HJLTFET and PNS-HJLTFET at $V_{ds}=1$ V.

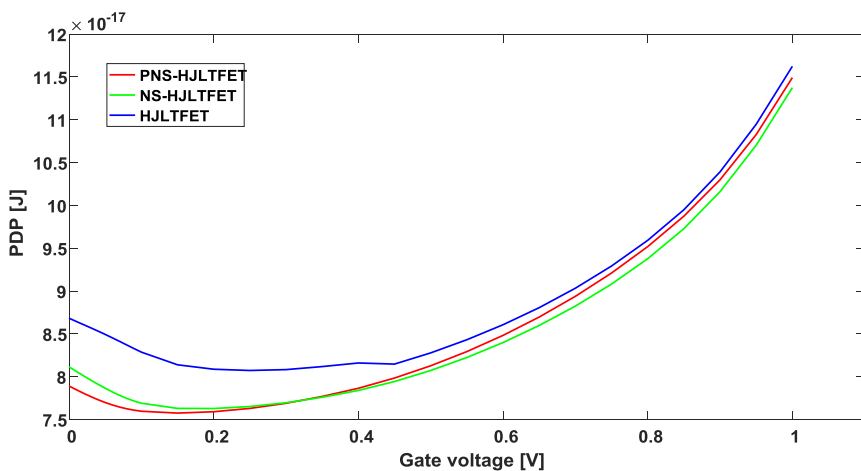


Fig. 13: Power-delay product (PDP) for HJLTFET, NS-HJLTFET and PNS-HJLTFET at $V_{ds}=1$ V.

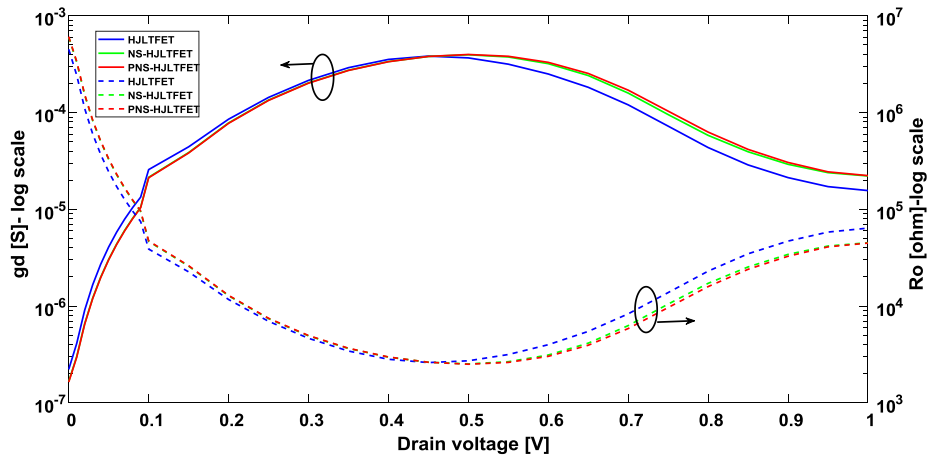


Fig. 14: Output conductance (left) and output resistance (right) for HJLTFET, NS-HJLTFET and PNS-HJLTFET at $V_{gs}=1V$.

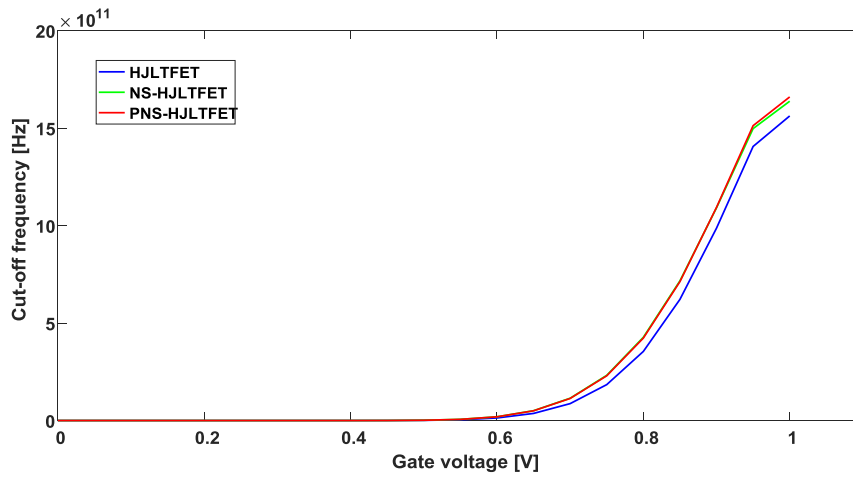


Fig. 15: Cut-off frequency for HJLTFET, NS-HJLTFET and PNS-HJLTFET [$V_{ds}=1V$].

CONCLUSION

In according to simulation results, the uncertainties arising from the manufacturing process affect the performance of JLTFT and HJLTFETs in analog and digital applications. Though the process variation is avoidable but our study showed this can be considered as an advantage. It have been shown uniform decrease of gate oxide thickness with the same slope from right to the left (ND-JLTFT and ND-HJLTFET) and from left to right (NS-JLTFT and NS-HJLTFET) changed device performance significantly. Due to the extracted curves, the NS-HJLTFET had the best state except to ambipolar current. Therefore a structure namely PNS-HJLTFET was proposed which uses an oxide pocket close to the drain. The simulation results showed the proposed structure

suppressed the ambipolar current while keeping other good performance.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this manuscript.

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