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ORIGINAL ARTICLE

Generic parity generators design using LTEx methodology: A quantum-dot cellular automata based approach

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Abstract

Quantum-dot Cellular Automata (QCA) is a prominent paradigm that is considered to continue its dominance in the computation at deep sub-micron regime in nanotechnology. The QCA realizations of five-input Majority Voter based multilevel parity generator circuits have been introduced in recent years. However, no attention has been paid towards the QCA instantiation of the generic (n-bit) even and odd parity generator. In this paper, a comprehensive QCA based methodology, termed as LTEx methodology is proposed to produce n-bit even and odd parity generators. The two-input Layered T Exclusive OR (LTEx) module is used to implement high fan-in parity generators. The corollaries first formulate the QCA design metrics such as O-Cost, $Cost_\alpha$ and irreversible power dissipation and then exploit the operability of the LTEx module to instantiate the efficient n-bit parity generators. These parity generators can exclusively be used in error detection and correction schemes.

Keywords: *$Cost_\alpha$; Layered T Gate; LTEx Module; Parity Generator; Quantum Cellular Automata (QCA)*

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INTRODUCTION

The limitations of conventional Complementary Metal Oxide Semiconductor (CMOS) based VLSI technology [1] lead the researchers' bias towards nanotechnology paradigm which has been revolutionized by the application of Quantum-dot Cellular Automata (QCA) [2] since last two years. In QCA, binary logic computation is possible without the application of traditional voltage and current flow. A Quantum Cell, the basic structure of QCA technology, contains four tiny semiconductor dots with two excess electrons. The positions of the excess electrons within the squared QCA cell define the logic state as either 1 or 0. The Columbic interactions among the array of QCA cells keep the information flowing within the circuit.

The extreme high packing density, ultra-high speed operation and extreme low power dissipation are the phenomenal features of this nanotechnology [3]. There are four basic types of QCA namely, Metal-dot QCA, Semiconductor QCA, Molecular QCA and Magnetic QCA [4-7]. The gallium arsenide based heterostructure semiconductor QCA technology and its related design parameters have been used in this work owing to the significant advancement in semiconductor fabrication technology in subnanometre regime [8-9].

After the experimental fabrication of coplanar silicon dangling bond based quantum-dots [10], researchers are now working on the multilayer structures of QCA [11].

However, some issues of concern with this technology still remain such as fabrication faults at the layout stage and input-output fixation with real time physical parameters [12].

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The error detection and correction codes are the contingent portion in binary data transmission networks [13]. The transmitted logic 0's and 1's may change their logic at the receiver end due to the presence of noise in the environment. The parity generators are inherent part for error detection and correction in the transceiver system [14-20].

The main aim of this work is focused on the generic design of even and odd parity generators by using the LTEx methodology [21-22] of QCA. In this methodology, the two-input LTEx module conforms to the Exclusive-OR output. Exclusive OR Gate is the key module of the parity generators, which are constructed using the two-input LTEx modules. After the successful instantiation of lower order parity generators, higher order parity generators are also proposed to be used in multi-level nano-communication circuits. The $Cost_{\alpha}$ analysis [22-23] of the proposed LTEx parity generator circuits is carried out with the best reported ones available in the literature to analyze the complexity and irreversible power dissipation that establishes the superiority of the proposed generator over the others.

This paper is organized as follows: Section 2 discusses the background of QCA. It shows the basic structures of QCA and retrospect's the QCA design metrics. Literature surveys are also presented here for the key parity generators available as of now. Section 3 introduces the layouts of parity generators by using Layered T Gate. A generic methodology to formulate the n-bit parity generator layouts for high fan-in multi-level QCA nano-communication circuits is proposed in this section. The comparison of parity generator designs of different bit length with the existing designs in terms of QCA design metrics are presented in Section 4. Finally, Section 5 concludes with the results.

COMPUTATIONAL METHODS

Basic structure of QCA circuits

The quantum cell comprises of four quantum dots placed at the corners of a square. Free electrons are located on two of those four diagonal dots. A single quantum cell is considered to form the computational elements with their interconnecting wires of a circuit as shown in Fig. 1(a), Quantum Cell, Polarization P. The orientation of electrons within the quantum cell corresponds to the binary representation of logic 1 or 0 as given in Fig. 1(b) P = +1 and 1(c) P = -1 respectively. An isolated quantum cell holds either of these two possible orientations which are called the ground states [5, 23]. Though a quantum cell is surrounded by the neighbor quantum cell, but tunneling is allowed only between the electrons. The electrons from the neighbor cells cannot tunnel as they fetch high inter-dot potential barrier.

The foremost logical structures formed by the electro-mechanically coupled quantum cells comprises of Binary Wire, conventional seven-cell inverter and the Majority Voter. The binary wire simply carries the information from one level to the next level of the QCA circuit. The Boolean inverter takes the input, inverts it and passes the same on to the output cell. The majority voter fetches the logic of the three inputs A, B and C. It decides the majority among these three logics and generates output Z in favour of the majority logic. Such computation of Majority Voter is validated by the equation Z = M (A, B, C) = AB + BC + CA. The structures of binary wire, conventional seven-cell inverter and Majority voter are shown in Figs. 2(a) Majority Voter, (b) Seven Cell Inverter and (c) Binary Wire respectively.

QCA clock

Every QCA circuit needs an external field, which is termed as QCA clock to control the flow of information [24]. This clock has four phases namely switch (phase 1), hold (phase 2), release (phase 3) and relax (phase 4) as mentioned in Fig. 3 QCA Clock Zone. The switch phase starts with unpolarized quantum cell and lower inter-dot potential barrier. Such barriers are increased and the quantum cell becomes polarized according to its previous cell's logic. At the end of this phase, the barriers attain maximum value that suppresses further intra-dot electron tunneling. As a result, the logic of the quantum cell becomes fixed. In the hold state, the barriers remain at a high state so that the quantum cell retains its polarization. The release phase starts decreasing the barriers and the quantum cell begins to relax. Finally, the relax phase pushes the cell to an unpolarized state.

Qca logic gate

Based on QCA technology, several researches have been done in the following computational reduction techniques such as: And-Or-Invert (AOI) Gate, Nand-Nor-Invert (NNI) Gate, Universal QCA Logic (UQCALG) Gate, Coupled Majority Voter

Minority (CMVMIN) Gate, FNZ Gate and Layered T Gate [21]. The biplanar-structure based Layered T Gate has been introduced to perform the universal NAND/NOR operation in QCA technology [22]. The rotated cell by using two-dimensional electron gases can implement the upper layer cells. The equation of Layered T Gate is given by equation (1):

$$\left.\begin{matrix} L_T^{+}(A,B) = \overline{AB} \text{ if fixed cell polarization } P+1 \\ L_T^{-}(A,B) = \overline{A+B} \text{ if fixed cell polarization } P=-1 \end{matrix}\right\} \quad (1)$$

Design metrics of QCA

The evaluation of QCA layout designs of digital circuits like adders, multiplexers, memories and other significant blocks of arithmetic logic unit is carried out in terms of the following points: (i) O-Cost, (ii) Effective area, (iii) $Cost_{\alpha}$ (iv) Irreversible Power Dissipation and (v) Complexity [23-24]. To obtain the most favourable QCA layout designs, the minimal value of above mentioned parameters are desirable. The definitions of these parameters are discussed below:

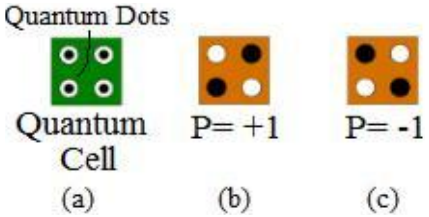

Fig. 1: a) Quantum Cell, Polarization P: b) P=+1, c) P=-1.

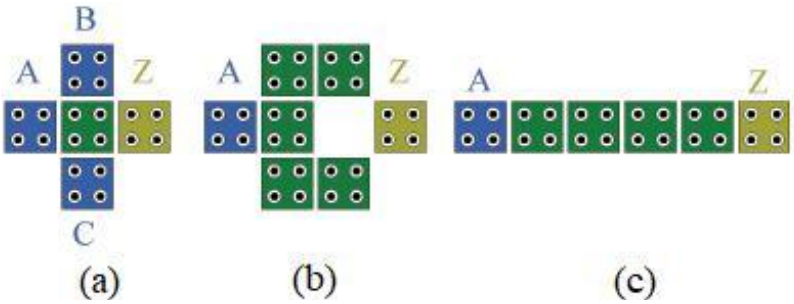

Fig. 2: a) Majority Voter, b) Seven Cell Inverter, c) Binary Wire.

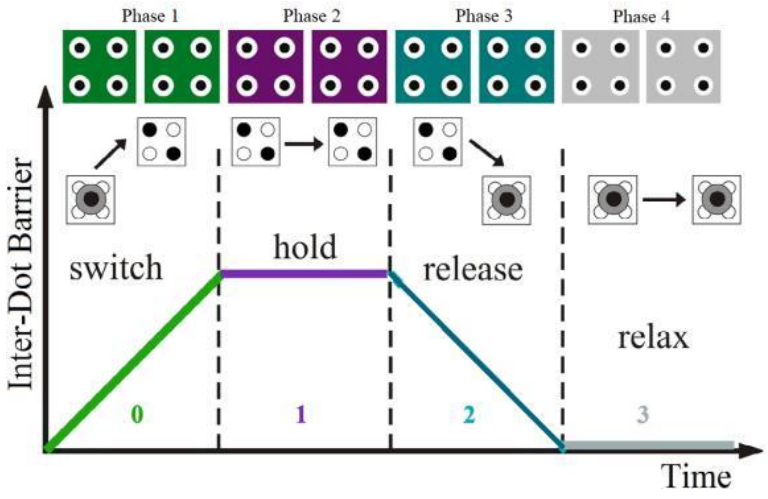

Fig. 3: QCA Clock Zone.

(i) O-Cost: The number of quantum cells in a specific QCA layout is termed as O-Cost [21-22, 25]. The QCA layout with lower value of O-Cost is the expected parameter to design an area-delay-power efficient circuit. For example, the two-input multiplexer of Fig. 4 has 67 quantum cells, making the value of the O-Cost to be 67 [26].

(ii) Effective Area: The total area of the QCA layout is called effective area. The rectangular box that covers 81648 nm^2 in Fig. 4 two inputs Multiplexer in [26] is the effective area for the specified two-input multiplexer.

(iii) $Cost_\alpha$: The QCA layout design metric that includes the performance, complexity, fabrication difficulty and irreversible power dissipation is called $Cost_\alpha$ [23]. The expression of the $Cost_\alpha$ is given by:

$$\mathrm{Cost}_\alpha = (\mathrm{M}^2 + \mathrm{I} + \mathrm{C}^2) * \mathrm{T} \quad (2)$$

In equation (2), M=number of Majority Voter, I=number of Inverter and C=Crossover. The value of M, I, C, T for two-input multiplexer of Fig. 4 become 3, 2, 2, 1 respectively. Hence the calculation for $Cost_\alpha$ becomes $(3^2+2+2^2)*1=15$. The value of C becomes 1 for a coplanar QCA layout but the multilayer structure makes C=3, as minimum three layers are needed above the main cell layer to make the layout operable [21-22].

(iv) Irreversible Power Dissipation: According to its definition [22], the term (M + I + C) becomes the Irreversible Power Dissipation in Majority Logic Synthesis. But for Layered T logic reduction technique, the term (L_T + I + C) counts Irreversible Power Dissipation.

(v) Complexity: The number of layer requirements in a QCA layout is complexity. As coplanar crossover is used in the layout of Fig. 3, the complexity C becomes 1.

Literature survey

Numerous research works have been published now; showcasing mostly the design of even parity generator structures such [14-20]. However, no work is reported so far for the design of generic odd parity generator. The implementation and metrics of all the existing works reported are summarized in Table 1. The existing designs use back to back three-input Majority Gate, inverter and five-input Majority Voter for carrying out parity generators and they may reduce the effective area and O-Cost of the generators considerably. But it may be mentioned that the structure of five-input Majority Gate is highly susceptible to cell displacement defects of QCA [27-29]. Moreover, the existing layouts of parity generators do not properly follow the design rules of QCA as mentioned in details in Table 1. The long QCA wires are abruptly placed in higher order parity generator layouts and "layout = timing" rule is not properly implemented in parity generator design.

The existing parity generators are solely implemented for the generation of even bit parity. Neither the guidelines nor the layouts of generic odd-parity generators are revealed from these available methodologies. Mostly the use of five-input Majority Gate requires additional three-input Majority Gate which increases the O-Cost and the circuit complexity as well. The "Cost" of five-input Majority Gate based QCA layout has not been analyzed yet. Serious issues in the design of existing parity generator layouts are:

(i) The "layout=timing" problem is not fixed.

(ii) Long QCA wires are placed in higher order parity generator circuits.

The rule for assigning minimum number of QCA cells under single clocking zone is not maintained in most of the cases.

LTEx parity generators

The parity generators designed with LTEx methodology are called the LTEx parity generators. To understand the LTEx methodology, it is necessary to introduce two-input LTEx Module as elaborated below.

Two-input LTEx module

The LTEx module of Fig. 5a, Block diagram includes four Layered T NAND (LT NAND) gates. The LT NAND1 takes two inputs A1 and A0 to produce intermediary output of T1 at clock 0. The inputs A1 and A0 are coupled separately with the intermediary output T1. Then T1 is connected to the input ports of LT NAND2 and LT NAND3 to produce second level intermediary outputs of T2 and T3 respectively at clock 1. These intermediary outputs of T2 and T3 are then given to LT NAND4 to get the final output Z0. The clock signals are applied to quantum cells in order of 0,1,2,3, so that the intermediary outputs get evaluated at clock 3 for proper Exclusive OR output generation. The detailed mathematical interpretations of LTEx block are given by equation (3) as follows:

$$\mathrm{Z0} = \mathrm{LTEx}(\mathrm{A1}, \mathrm{A0}) = \mathrm{T}_\mathrm{L}^+((\mathrm{A1}, \mathrm{T}_\mathrm{L}^+(\mathrm{A1}, \mathrm{A0}), (\mathrm{A0}, \mathrm{T}_\mathrm{L}^+(\mathrm{A1}, \mathrm{A0}))) \quad (3)$$

Equation (3) is commonly used in LTEx

methodology to design even and odd parity generator QCA layouts. The output of the two-input LTEx module is shown in figure 6 Output of two-input LTEx module.

The n-bit even parity generator produces Ex-ORed operation of inputs as P_even = A[n-1] ⊕ A[n-2] ⊕ A[n-3] ⊕ ... ⊕A[2] ⊕A[1] ⊕A[0] and stores it in P_Even. To implement the Ex-ORed addition of such inputs in parity generators, the two-input LTEx modules are required. Primarily, the most significant two bits i.e. A[n-1] and A[n-2] are Ex-ORed by using the first LTEx module. After that the intermediary result is further Ex-ORed with A[n-3] by using second level LTEx module. This process continues till it ends up with the ultimate Ex-OR result of A[1] ⊕A[0] which requires (n-1) number of LTEx modules.

Unlike the even counterparts, the term A[n-1] ⊕ A[n-2] ⊕ A[n-3] ⊕ ... ⊕A[2] ⊕A[1] ⊕A[0] is inverted to form P_odd. Total (n-1) numbers of two-input LTEx modules are used to obtain the expected output of P_odd. The LTEx methodology to generate n-bit even/odd parity generator layouts is given by Algorithm 1:

Algorithm 1: LTEx Methodology:

Step 1: Follow the LTEx expression as follows in expression (3) to find the intermediary result A[i] ⊕ A[j] LTEx(A[i],A[j])=T_L^+ ((A[i],T_L^+ (A[i],A[j]), (A[j],T_L^+ (A[i],A[j])))
where i, j varies from 0-1.

Step 2:

If even parity generator layout is to be generated then,

P_even=LTEx(A[n-1],LTEx(A[n-1],A[n-2])),... LTEx(A[2], LTEx(A[1], A[0]))

else

P_odd=LTEx(A[n-1],LTEx(A[n-1],A[n-2])), ...LTEx(A[2], LTEx(A[1], A[0]))

According to LTEx methodology, the QCA design parameters such as O-Cost, $Cost_{\alpha}$, Complexity, Irreversible Power Dissipation of even and odd parity generators are modelled in Corollaries 1-8 as provided in Table 2.

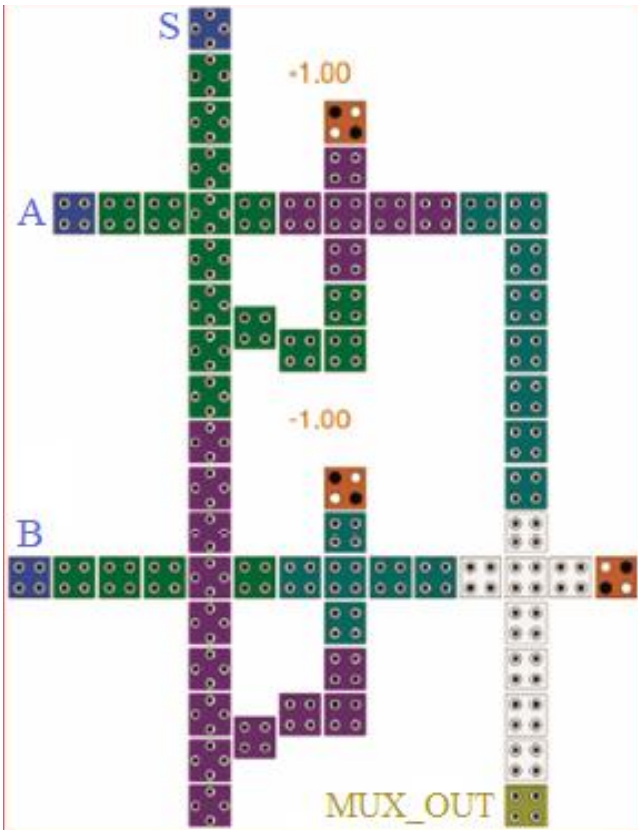

Fig. 4: Two input Multiplexer in [26].

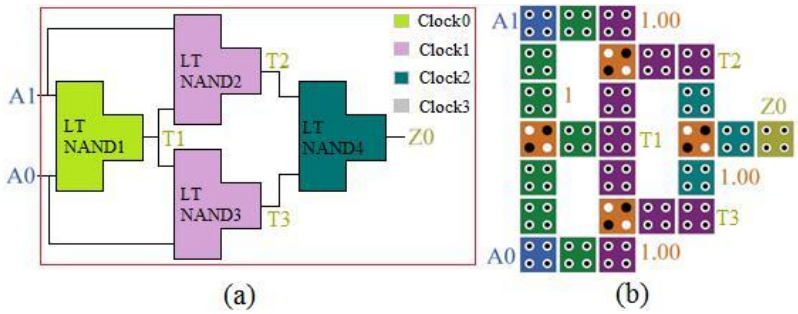

Fig. 5: a) Block diagram and b) QCA Layout of Two-input LTEx module.

Table 1: A Comparative Summary of the Existing QCA parity generators.

Design	Reference Paper	Main Idea	Advantages	Limitations
even parity generators	In [14]	The 4, 8, 16 and 32-bit even parity generators are proposed using conventional three-input Majority Gate based Ex-OR Gate.	• New guideline to design higher order even parity generators are introduced • Modular approach	• Does not provide any approach to generate odd parity generators. • Random coplanar crossovers are placed within the layouts • Long QCA wires are used which may cause loss of energy level during data propagation • Area-Delay product is not optimized
even parity generators	In [15]	The 4,8, 16 and 32-bit even parity generators are proposed using a novel five-input Majority Gate based Ex-OR Gate. The logical design involves Sum-of Products.	• Five-input Majority Gate eases the generation of higher order parity generators • Reduced effective area • Improved Latency • Modular approach and extendable	• High O-Cost • Design rules of clock zone assignments are not followed. Rule for minimum number of QCA cell under single clocking zone is not properly followed • The approach to generate odd parity generators are not provided
even parity generators	In [16]	Proposing 4, 8, 16 and 32-bit even parity generators using modified design of five-input Majority Gate based Ex-OR Gate. Power dissipation is also carried out for proposed layouts.	• High packing density • Reduced effective area • Reduced O-Cost • Uniform number of Input bits-Delay relationship • Power dissipation analysis has been carried out for parity generator circuits • Modular approach and extendable	• The presence of corner QCA cells in the modified layout of Ex-OR gate is prone to fabrication faults • Design rule for clocking minimum QCA cells in a single clock zone is not followed • One additional three-input Majority Gate at each level makes number of gate higher • The approach to generate odd parity generators are not provided
even parity generators	In [17]	Energy dissipation analysis based 4, 8, 16 and 32-bit even parity generators are proposed using modified design of five-input Majority Gate.	• High degree of packing density • O-Cost is less • Modular approach and extendable	• Changing design rules [30]
even parity generators	In [18]*	Proposing 4,8, 16 and 32-bit even parity generators using five-input Majority Gate.	• Reduced effective area • Reduced O-Cost • Reduced latency	• Design rules are not followed • $\neq 2^n$-bit parity generator design is not possible • The approach to generate odd parity generators are not provided
even parity generators	In [19]	Proposing 4,8, 16 and 32-bit even parity generators using rotated three-input Majority gate and novel five-input Majority gate based Exclusive OR Gate.	• Modular approach and extendable • Variation of output polarization versus change in temperature has been addressed	• Delay is higher than the previous designs • Input-output bits are abruptly placed within the circuits • Critical delay path can be observed in high fan-in parity generator circuits
even parity generators	In [20]	Proposing only 4-bit Parity Generator layout which uses 3-input Majority Gate based Ex-OR gate has been reported.	• Modular approach • Power dissipation analysis has been shown using QCAPro tool [31] • Higher order parity checker and full adder layouts have been considered to show the scalability of the proposed Ex-OR gate.	• The Cost calculation for generic parity generator, parity checker is not given. • High degree precision during the fabrication is required otherwise proposed Ex-OR gate may not work. • The guidelines to generate 2^n-bit parity generator is missing

*Bahar parity generator is not considered due to the serious issues of its design rules

IMPLEMENTATION OF N-BIT PARITY GENERATORS USING LTEx METHODOLOGY

Even parity generators

Even and odd Parity Generators are implemented in this sub-section according to the proposed LTEx Methodology. As an example of four-bit even parity generator, the inputs *i.e.* A3 and A2 are Ex-ORed at the third clock zone to generate the intermediary output as shown in Fig. 5a Block diagram. The EX-ORed output of A3 and A2 is further EX-ORed with A1 at the second level and the second intermittent output is finally Ex-ORed with A0 to produce P_even as demonstrated in Fig. 7a QCA Layouts of LTEx even Parity Generators generated using LTEx Methodology: (a) 4-bit. The QCA layout of four bit parity generator consumes 0.09 μm^2 effective area, employs 78 quantum cells and is indicating the O-Cost as 78 and generates P_even with QCA clock delay of 2.25.

Higher orders of even parity generator can also be generated implementing the proposed LTEx methodology. The eight-bit even parity generator of Fig. 6b QCA Layouts of LTEx even Parity Generators generated using LTEx Methodology: (b) 8-bit requires (8-1) =7 two-input LTEx module. Similarly, the 16-bit and 32-bit even LTEx parity generators need (16-1) =15 and (32-1) =31 two-input LTEx module respectively as demonstrated in Fig. 6b-d. In general for the design of n-bit even parity generators, the requirement is (n-1) cascaded two-input LTEx modules.

The O-Cost for 8-bit LTEx parity generator is 26*(8-1) = 182 whereas the 16-bit and 32-bit LTEx parity generators have O-Cost of 26*(16-1) = 390 and 26*(32-1)= 806 respectively. So the O-Cost of 26*(n-1) can be presumed for an n-bit even LTEx parity generator. The value of $Cost_\alpha$ for four-input layout of Fig. 7a QCA Layouts of LTEx even Parity Generators generated using LTEx Methodology: (a) 4-bit becomes $(6^2+6+3^2)*2.25=114.75$. Similarly the $Cost_\alpha$ for 8-bit, 16-bit & 32-bit LTEx counterparts of Figs. 7b-d QCA Layouts of

Table 2: QCA Design Parameters of n-bit even LTEx parity generators.

	Corollary for even parity generator		Corollary for odd parity generator
1)	For an n-bit LTEx even parity generator, the O-Cost is 26*(n-1) for n≥2.	5)	For an n-bit LTEx odd parity generator, the O-Cost is 26*n-24 for n≥2.
2)	For an n-bit LTEx even parity generator, the Delay is 0.75*(n-1) for n≥2.	6)	For an n-bit LTEx odd parity generator, the Delay is 0.75*(n-1) for n≥2.
3)	For an n-bit LTEx even parity generator, the $Cost_\alpha$ is $\left\{\left(\frac{3*n^2}{2}\right)+\left(\frac{3*n}{2}\right)+3^2\right\}*0.75*(n-1)$ for n≥2.	7)	For an n-bit LTEx odd parity generator, the $Cost_\alpha$ is $\left\{\left(\frac{3*n^2}{2}\right)+\left(\frac{3*n}{2}+1\right)+3^2\right\}*0.75*(n-1)$ for n≥2.
4)	For an n-bit LTEx even parity generator, the Irreversible Power Dissipation is 3*n+3 for n≥2.	8)	For an n-bit LTEx odd parity generator, the Irreversible Power Dissipation is 3*n+5 for n≥2.

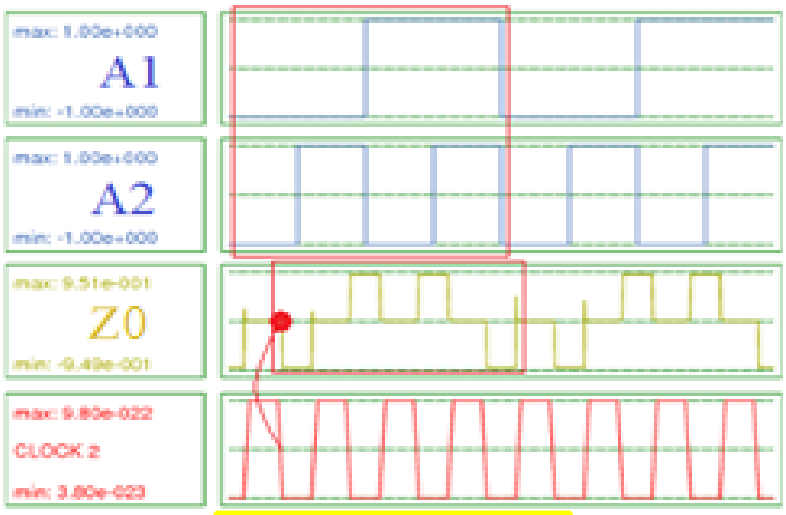

Fig. 6: Output of two-input LTEx module.

LTEx even parity generators generated using LTEx methodology: (b) 8-bit, (c) 16-bit and (d) 32-bit may be counted as $(14^2+14+3^2)*5.25= 1118.25$, $(30^2+30+3^2)*11.25= 10563.75$ & $(62^2+62+3^2)*22.25= 87108.75$ respectively. The generic expression for an n-bit odd parity generator is $\left\{\left(\frac{3*n^2}{2}\right)+\left(\frac{3*n}{2}\right)+3^2\right\}*0.75*(n-1)$.

Odd parity generators

It can be observed from LTEx Methodology that inversion of P_even generates P_odd. This observation has made the instantiations of odd parity generator easier. The inverters at the end of the even parity bit QCA layouts do definitely generate odd parity counterparts. The 4-bit, 8-bit, 16-bit and 32-bit QCA odd parity generator's layouts are demonstrated in Fig. 8(a)-(d) QCA Layouts of LTEx odd Parity Generators generated using LTEx Methodology: (a) 4-bit, (b) 8-bit, (c) 16-bit and (d) 32-bit. The number of LTEx modules for odd parity layouts will remain same as their even counterparts. As two quantum cells are required to invert the even parity output P_even, so the O-Cost values will differ by a count of 2. As an example for 4-bit odd parity layout, the O-Cost becomes 26+2=28 as shown in Fig. 8(a) QCA Layouts of LTEx odd Parity Generators generated using LTEx Methodology: (a) 4-bit. Similar increment of 2 in O-Cost can be observed in 8-bit, 16-bit and 32-bit odd parity layouts and the respective calculations are as follows : (182+2)=184, (390+2)=392 and (806+2)=808. The effective area of 4-bit, 8-bit, 16-bit and 32-bit odd parity generators are reported as 0.08 μm^2 , 0.27 μm^2, 0.89 μm^2 and 3.23 μm^2 respectively. The $Cost_\alpha$ for 4-bit odd parity generator is calculated as $(6^2+7+3^2)*2.25= 117$.

Since an additional inverter is required to invert P_even, so the number of inverter for the 4-bit odd parity generator becomes 6+1=7. The calculations of $Cost_\alpha$ for 8-bit, 16-bit and 32-bit odd counterparts are calculated as follows: $(14^2+15+3^2)*5.25= 1155$, $(30^2+31+3^2)*11.25= 10575$, $(62^2+63+3^2)*22.25= 87131$ respectively. The generic expression for $Cost_\alpha$ of an n-bit odd parity generator is $\left\{\left(\frac{3*n^2}{2}\right)+\left(\frac{3*n}{2}+1\right)+3^2\right\}*0.75*(n-1)$.

The irreversible power dissipation for LTEx QCA layouts is modelled as $\{L_T+(I+1)+C_{ml}\}$. For an n-bit odd parity generator, this factor becomes $(\frac{3*n}{2}+(\frac{3*n}{2}+1)+3) = (3*n+5)= (3*n+5)$. The delays of LTEx even and odd parity generators have similar clock delay of 0.75*(n-1). The Power Delay Products of n-bit even and odd parity generators are as same as (3*n+3)*0.75*(n-1) = 3.75*n-2.25. The QCA design parameters of proposed 4-bit, 8-bit, 16-bit and 32-bit even and odd parity generators are summarized in Table 3.

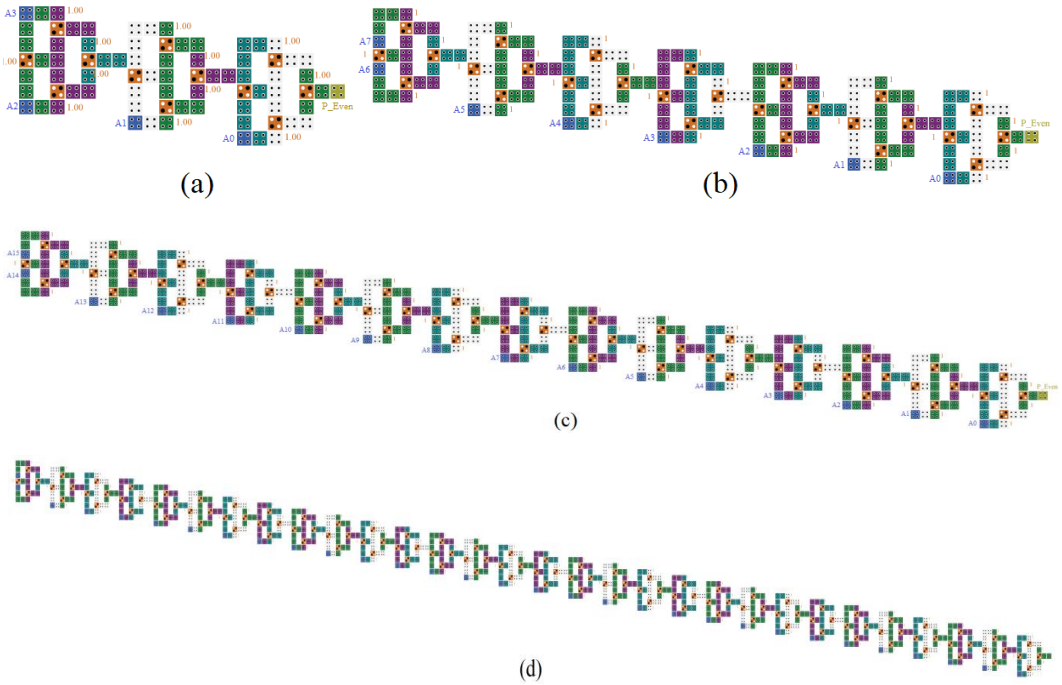

Fig. 7: QCA Layouts of LTEx even parity generators generated using LTEx methodology: a) 4-bit, (b) 8-bit, c) 16-bit and d) 32-b.

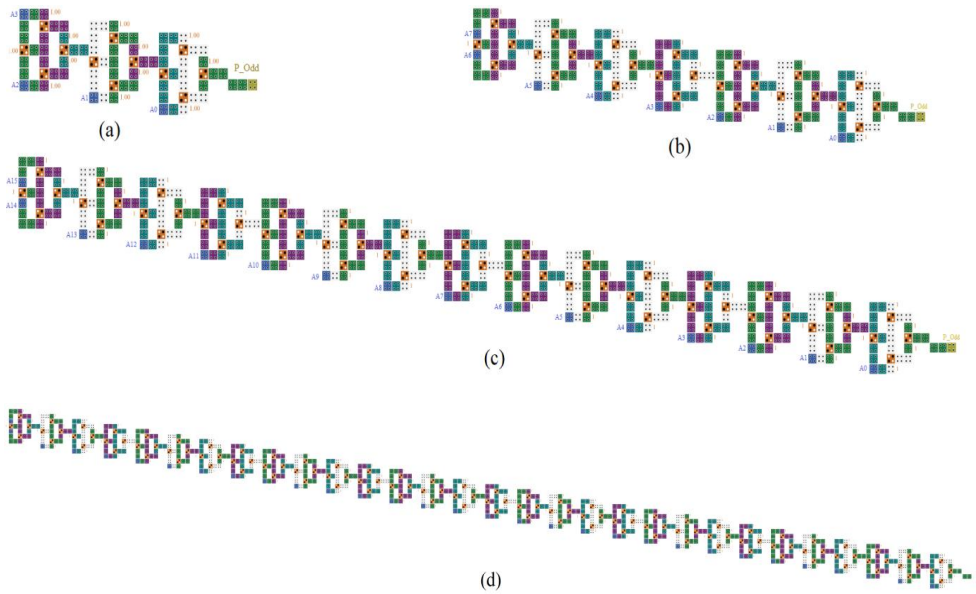

Fig. 8: QCA Layouts of LTEx odd parity generators generated using LTEx methodology: a) 4-bit, (b) 8-bit, c) 16-bit and d) 32-bit.

Table 3: Summary of QCA design parameters of n-bit even LTEx parity generators.

Sl No.	Design of parity generator	O-Cost	Effective Area in μm^2	$Cost_\alpha$	Irreversible Power Dissipation
1	4-bit even	78	0.074	114.75	15
2	8-bit even	182	0.267	1118.25	27
3	16-bit even	390	0.808	10563.75	51
4	32-bit even	806	2.07	87108.75	99
5	4-bit odd	80	0.081	117	16
6	8-bit odd	184	0.276	1155	28
7	16-bit odd	392	0.922	10575	52
8	32-bit odd	808	2.17	87131	100

RESULTS AND DISCUSSION

This work proposes LTEx methodology to implement generic even and odd parity generators by using the Layered T Gate based Exclusive OR Gate [21].The output of two-input LTEx module is verified in Fig. 6 Output of two-input LTEx module. At the falling edge of clock 2, the output Z0 conforms the Ex-OR output. The corollaries 1-8 of LTEx methodology mentioned in Table 2 provide clear ideas about the requirement of LTEx modules, O-Cost, Latency, $Cost_\alpha$ and Irreversible Power Dissipation during the realization of generic LTEx parity generators. From tables 2 and 3, it can be observed that 4-bit, 8-bit, 16-bit and 32-bit odd LTEx parity generators need 2.56%, 1.09%, 0.51% and 0.24% additional O-Cost respectively than

that of their even counterparts.

Comparison of proposed even and odd LTEx parity generators in terms of effective area in μm^2 shows respective increase of 9.45%, 3.37%, 14.10% and 4.83% in 4-bit, 8-bit, 16-bit and 32-bit odd LTEx parity generator's respective area compared to their even counterparts. The $Cost_\alpha$ for 4-bit, 8-bit, 16-bit and 32-bit odd LTEx parity generators are 2.63%, -3.19%, 0.106% and 0.0255% higher than that of their even LTEx counterparts as reported in the table 3. The 4-bit, 8-bit, 16-bit and 32-bit odd LTEx parity generators consume 6.67%, 3.70%, 1.96% and 1.01% respective higher power compared to their even LTEx counterparts as summarized in table 3. As the LTEx modules are using a single additional layer, so the complexity becomes 3 for the proposed LTEx layouts.

The proposed 4-bit, 8-bit, 16-bit and 32-bit even LTEx parity generators are compared with the existing designs of [14-20] in terms of O-Cost, Effective Area in nm^2, $Cost_\alpha$ and Irreversible Power Dissipation. The 4-bit LTEx parity generator requires 10.34% less O-Cost than the optimized 4-bit Singh parity generator counterpart [17]. The 4-bit LTEx parity generator consumes sharp 24% less effective area than the Singh counterpart [17] and Sasamal counterpart [19]. Till date, the 4-bit Hashemi parity generator [14] has been reported as the best design in terms of $Cost_\alpha$ and Irreversible Power Dissipation. However the $Cost_\alpha$ for 4-bit LTEx parity generator is counted as 114.75 in Table 4 whereas the value becomes 220 for the Hashemi parity generator [14]. On the other hand, the Irreversible Power Dissipation becomes 16 for the former parity generator [14]. Hence sharp 47.84% reduced value of $Cost_\alpha$ and 6.25% less power consumption in comparison to Hashemi 4-bit parity generator [14] can be noted from Table 4.

The 8-bit LTEx parity generator requires 14.56% less O-Cost and 11% reduced effective area as compared to 8-bit Singh parity generator design [17]. Like the 4-bit LTEx Parity Generator, the 8-bit LTEx parity generator also has 38.42% less $Cost_\alpha$ and ~20.6% reduced Power consumption as compared to the Hashemi 8-bit parity generator [14] as shown in Table 4.

In case of the 16-bit parity generator design, the proposed QCA layout has 18.75% less O-Cost and it covers 0.25% less effective area than its competitor, namely the Singh parity generator [17] and Sasamal counterpart [19]. The 16-bit LTEx parity generator has become favourable due to its 2.13% lesser $Cost_\alpha$ and 32.9 % reduced power consumption than Hashemi counterpart [14] as summarized in Table 4. The 32-bit Singh parity generator has best QCA design metrics in terms of its O-Cost and effective area among the Anghizi parity generator [15], the Sheikhfaal parity generator [16] and the Hashemi parity generator [14] because this generator employs the design of Ex-OR Gate with five-input Majority Voters in the high fan-in QCA layouts. The successful instantiation of the 32-bit LTEx parity generator makes it better even compared to Singh counterpart [17]. The 32-bit LTEx parity generator leads by 22.8% O-Cost and 0.49% effective area than Singh parity counterpart [17]. Moreover the 32-bit LTEx parity generator consumes 33.29% less irreversible power than Anghizi parity generator [15].

A.N. Bahar *et al*. [18] have proposed another five-input Majority Voter based even parity generators. The Bahar parity generator needs additional interconnects because the input and outputs are placed inside the inner part of the QCA layouts. Hence the design rule of QCA is not followed. The corner cells of five-input Majority Gates are highly sensitive to QCA defects like Cell Displacement defect, Cell Misalignment defect and Rotational cell defects [27-29]. In addition, the formulation of ≠ 2 -bit Bahar parity generator using five-input Majority Gate is critical. Due to these serious issues, this work excludes the parameters of Bahar parity generator from the evaluation of proposed LTEx parity generators. It is thus evident that the LTEx methodology clearly estimates the requirements of LTEx module, delay, O-Cost, $Cost_\alpha$, Irreversible Power Dissipation of generic even, and odd LTEx parity generators Table 2 whereas, the previous designs neither proposed odd parity generator nor provide such estimations of n-bit parity generators as the best of author's knowledge. Though LTEx parity generators show high delay compared to the existing designs, still the proposed parity generators excel in cost function as shown in table 4. Moreover the proposed layouts have the following features:

(i) The input-output cells are placed at the border of the layouts to avoid unnecessary delay.

(ii) Minimum two cells are clocked together to ensure the proper dataflow through the circuit.

(iii) The use of QCA cells with +1/-1 orientation makes the layouts more stable [30].

Table 4: Comparison summary of even parity generators [14-17, 19-20] with proposed LTEx even counterparts.

Sl. No.	Design Proposed	No. of Bits	O-Cost	Effective Area in μm^2	Delay	$Cost_\alpha$	Irreversible Power Dissipation	Layout Type
1.	In [14]	4	168	0.28	2.75	220	16	Coplanar
		8	408	0.8	4	1816	34	
		16	912	2.09	5.25	10794	76	
		32	1968	5.16	6.5	91476	156	
2.	In [15]	4	188	0.20	2.75	1390.59	27.8	Coplanar
		8	369	0.49	4	5546.61	54.6	
		16	847	1.46	5.25	15228.07	81.4	
		32	1862	3.58	6.5	9122.08	148.4	
3.	In [16]	4	98	0.11	2	2781.68	46.2	Coplanar
		8	241	0.37	3	22647.72	101.8	
		16	537	1.04	4	138508	217	
		32	1167	2.67	5	624772.8	447.4	
4.	In [17]	4	87	0.10	1.75	2433.97	41.2	Coplanar
		8	213	0.30	2.75	10601.25	73	
		16	480	0.81	3.75	46775.85	130.6	
		32	1044	2.08	4.75	211240.3	245.8	
5.	In [19]	4	97	0.1	1.75	445.20	49.98	Coplanar
		8	235	0.3	2.75	3039.87	107.1	
		16	523	0.81	3.75	16621.85	221.34	
		32	1126	2.1	4.75	87834.30	386.82	
6	In [20]	4	159	0.26	3	382.4	122	Coplanar
		8	NA*	NA	NA	NA	NA	
		16	NA	NA	NA	NA	NA	
		32	NA	NA	NA	NA	NA	
7	Proposed LTEx parity generators	4	78	0.074	2.25	114.75	15	Biplanar Alternative Structure
		8	182	0.267	5.25	1118.25	27	
		16	390	0.808	11.25	10563.75	51	
		32	806	2.07	23.25	87108.75	99	

*NA=NOT AVAILABLE

The fabrication of two-input LTEx module can be done by biplanar alternative cells [11]. As biplanar alternative cells are not true three-dimensional structure, so the complexity of fabrication of three-dimensional structure can be taken aside. The upper layer cells of Fig. 5(b) QCA Layout of Two-input LTEx module can be implemented by rotated cell using two-dimensional electron gases. Moreover, in terms of QCA design metrics the biplanar approach of the proposed layouts makes the methodology effective.

The outputs of LTEx parity generators have been demonstrated in Fig. 9(a)-(h) Output of even parity generator (a) 4-bit, (c) 8-bit, (e) 16-bit, (g) 32-bit and odd parity generator (b) 4-bit, (d) 8-bit, (f) 16-bit, (h) 32-bit. The outputs of proposed LTEx parity generator layouts are producing the necessary result at clock 0. Hence the falling edge of clock 0 plays pivotal role in obtaining the proper output as demonstrated by using rectangular box in the Fig. 9(a)-(d). Similar case studies are also observed for 16-bit and 32-bit parity generator's outputs.

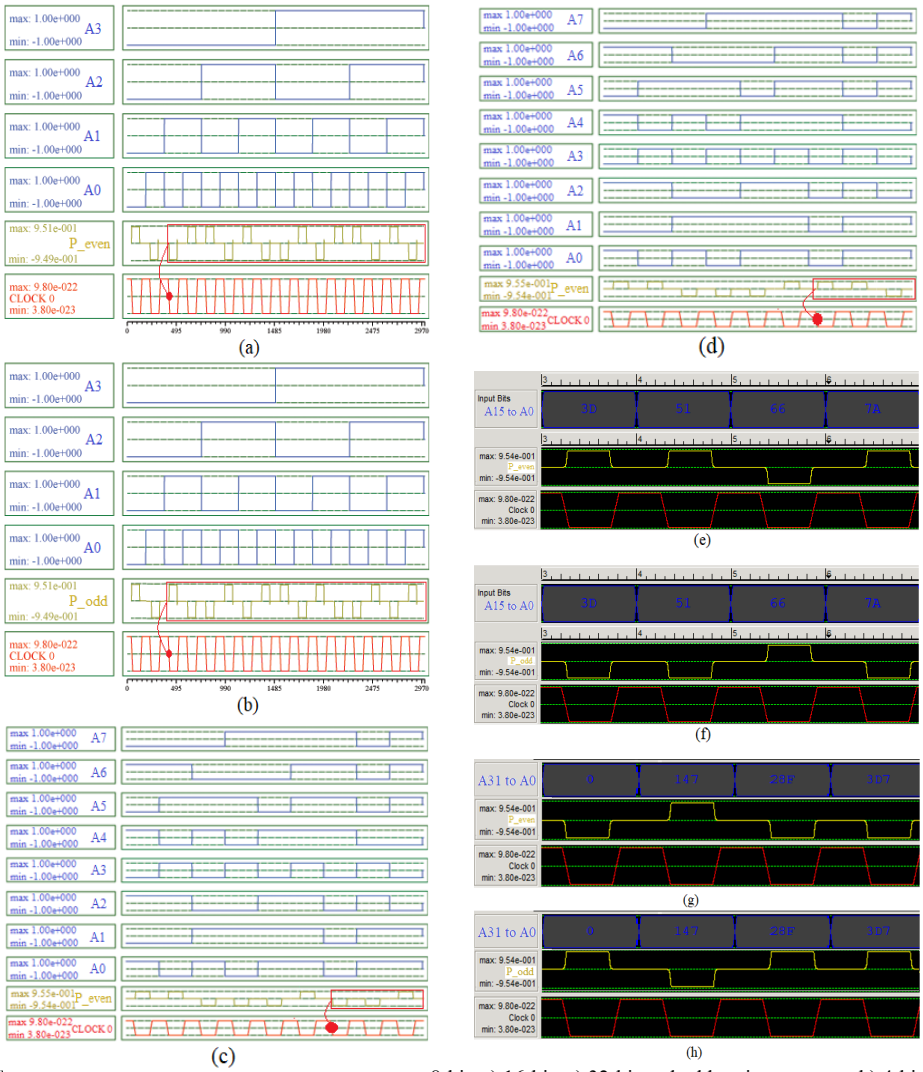

Fig. 9: Output of even parity generator a) 4-bit, c) 8-bit, e) 16-bit, g) 32-bit and odd parity generator b) 4-bit, d) 8-bit, f) 16-bit, h) 32-bit.

CONCLUSION

In this work, a new LTEx methodology is introduced which generates n-bit even and odd Parity generators. As the proposed algorithm uses two-input LTEx Module, the implemented parity generators are termed as LTEx parity generators. The significant contribution of this approach of LTEx methodology is the reduction of O-Cost, Effective Area, $Cost_{\alpha}$ and Irreversible Power Dissipation of QCA parity generator layouts. The even and odd parity generator layouts of different word sizes (*i.e.* 4, 8, 16 and 32) are generated by using well-known computer aided design tool QCADesigner. These layouts are compared with the existing designs for continuous research and development. Recurring and dynamic analysis of the comparative results may be significant for extending future research on this area.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this manuscript.

REFERENCES

[1] International Technology Roadmap for Semiconductors 2.0. (ITRS), 2015 Ed. Available: *www.semiconductors.org//* (Accessed 12 February 2018).

[2] Almatrood A. F., Singh H., (2015), Design of generalized pipeline cellular array in quantum-dot cellular automata. *IEEE Comput. Archit. Lett.* 14: 1-4.

[3] Macucci M., (2010), Quantum Cellular Automata. *Nanotech.* 4: 329–362.
[4] Amlani I., Orlov A., Toth G., Bernstein G. H., Lent C. S., Snider G. L., (1999), Digital logic gate using quantum-dot cellular automata *Science*. 284: 289-291.
[5] Toth G., Lent C., (2000), Quantum computing with quantum-dot cellular automata. *Phys. Rev. A*. 63: 1-9.
[6] Lent C., Isaksen B., Lieberman M., (2003), Molecular quantum-dot cellular automata. *J. Am. Chem. Soc.* 125: 1056-1063.
[7] Cowburn R., Welland M., (2000), Room temperature magnetic quantum cellular automata. *Science.* 287: 1466-1468.
[8] Amlani I., Orlov A. O., Kummamuru R. K., Bernstein G. H., Lent C. S., Snider G. L., (2000), Experimental demonstration of a leadless quantum-dot cellular automata cell. *Appl. Phys. Lett.* 77: 738-740.
[9] Farazkish R., (2018), Novel efficient fault-tolerant full-adder for quantum-dot cellular automata. *Int. J. Nano. Dimens.* 9: 58-67.
[10] Dilabio G. A., Wolkow R. A., Pitters J. L., Piva G., (2015), Atomistic quantum dots. *US Patent: US2015/0060771-A1*.
[11] Gin A., Tougaw P. D., Williams S., (1999), An alternative geometry for quantum-dot cellular automata. *AIP J. Appl. Phys.* 85: 8281-8286.
[12] Shukla S. K., Bahar R. I., (2007), Nano, quantum and molecular computing: Implications to high level design and validation. *Kluwer Academic Publishers*. ISBN 9781402080685.
[13] Kartalopoulos S. V., (2004), Error detection and correction codes in optical bit error rate: An estimation methodology. *Wiley-IEEE Pres*. ch9.
[14] Hashemi S., Farazkish R., Navi K., (2013), New quantum dot cellular automata cell arrangements. *J. Comput. Theor. Nanosci.* 10: 798–809.
[15] Angizi S., Alkaldy E., Bagherzadeh N., Navi K., (2014), Novel robust single layer wire crossing approach for exclusive or sum of products logic design with quantum-dot cellular automata. *J. Low Power Electron.* 10: 259-271.
[16] Sheikhfaal S., Angizi S., Sarmadi S., Moaiyeri M., Sayedsalehi S. H., (2015), Designing efficient QCA logical circuits with power dissipation analysis. *Microelectron. Eng.* 10: 462-471.
[17] Singh G., Sarin R. K., Raj B., (2016), A novel robust exclusive-OR function implementation in QCA nanotechnology with energy dissipation analysis. *J. Comput. Electron.* 15: 455-465.
[18] Bahar A. N., Uddin M. S., Abdullah-Al-Shafi M., Rahman Bhuiyan M. M., Ahmed K., (2017), Designing efficient QCA even parity generator circuits with power dissipation analysis. *Alexandria Eng. J.* Article In Press.
[19] Sasamal T. N., Singh A. K., Ghanekar U., (2018), Design and analysis of ultra-low power QCA parity generator circuit, In: Garg A., Bhoi A., Sanjeevikumar P., Kamani K. (eds) Advances in Power Systems and Energy Management. Lecture Notes in Electrical Engineering. 436: 347-354. Springer, Singapore.
[20] Kassa S. R., Nagaria R. K., Karthik R., (2018), Energy efficient neoteric design of a 3-input majority gate with its implementation and physical proof in quantum dot cellular automata. *Nano Communic. Networks.* 15: 28-40.
[21] Mukherjee C., Sukla S. S., Basu S. S., Chakraborty R., De D., (2015), Layered T full adder using quantum-dot cellular automata. *IEEE Int. Conf. Electronics, Comp. Communic. Technol.* 1-6.
[22] Mukherjee C., Panda S., Mukhopadhyay A. K., Maji B., (2017), Synthesis of standard functions and generic Ex-or Gate using layered T Gate. *Int. J. High Perform. Syst. Archit.* 7: 70-86.
[23] Liu W., Lu L., O'Neil M., Swartzlander E. E., (2014), A first step toward cost functions for quantum-dot cellular automata designs. *IEEE Trans Nanotechnol.* 13: 476-487.
[24] Campos C. A. T., Marciano A. L., Vilela Neto O. P., Torres F. S., (2016), USE: A universal, scalable, and efficient clocking scheme for QCA. *IEEE Trans. Comput. Aided. Design Integ. Circuits Sys.* 35: 513-517.
[25] Mukherjee C., Roy S. S., Panda S., Maji B., (2016), T-Gate: Concept of partial polarization in Quantum Dot Cellular Automata, *20th Int. Symp. VLSI Design and Test (VDAT)*. Guwahati, 1-6.
[26] Mardiris V. A., Karafyllidis I. G., (2010), Design and simulation of modular 2^n to 1 quantum-dot cellular automata (QCA) multiplexers. *Int. J. Circ. Theory Appl.* 38: 771–785.
[27] Sen B., Nath R. K., Mukherjee R., Sahu Y., Sikdar B. K., (2016), Towards designing reliable universal QCA logic in the presence of cell deposition defect. *29th Int. Conf. VLSI Design (VLSID)*, Kolkata. 575-576.
[28] Yang X., Cai L., Wang S., Wang Z., Feng C., (2012), Reliability and performance evaluation of QCA devices with rotation cell defect. *IEEE Trans. Nanotechnol.* 11: 1009-1018.
[29] Javid M., Mohamadi K., (2009), Characterization and tolerance of QCA full adder under missing cells defects. *2009 Fifth Int. Conf. MEMS NANO, and Smart Systems, Dubai, United Arab Emirates.* 85-88.
[30] Liu W., Lu L., O'Neill M., Swartzlander E. E., (2011), Design rules for quantum-dot cellular automata. *IEEE Int. Sympos. Circuits and Systems (ISCAS), Rio de Janeiro*. 2361-2364.
[31] Srivastava S., Asthana A., Bhanja S., Sarkar S., (2011), QCAPro-An error-power estimation tool for QCA circuit design. *IEEE Int. Sympos. Circuits and Systems (ISCAS), Rio de Janeiro.* 2377-2380.