

Novel attributes of steep-slope staggered type heterojunction p-channel electron-hole bilayer tunnel field effect transistor

Zahra Ahangari*

Department of Electronic, Faculty of Electrical Engineering Yadegar-e-Imam Khomeini (RAH), Shahr-e-Rey Branch, Islamic Azad University, Tehran, Iran.

Received 17 April 2019; revised 06 June 2019; accepted 08 June 2019; available online 12 June 2019

Abstract

In this paper, the electrical characteristics and sensitivity analysis of staggered type *p*-channel heterojunction electron-hole bilayer tunnel field effect transistor (HJ-EHBTFT) are thoroughly investigated via simulation study. The minimum lattice mismatch between InAs/GaAs_{0.1}Sb_{0.9} layers besides low carrier effective mass of materials provides high probability of tunneling current that eventually boosts the device performance. Unlike the conventional lateral tunnel field effect transistor (TFET), band to band tunneling (BTBT) in HJ-EHBTFT occurs in the electrically doped intrinsic channel and in the vertical direction which may considerably improve the on-state current. Due to the abrupt BTBT and steep transition from the off-state to on-state, subthreshold swing of 2mV/dec with on/off current ratio of 3.85×10^{13} is obtained. The sensitivity of main electrical parameters is computed via calculating their related standard deviation and mean values with respect to the variation of device critical design parameters. The 2D variation matrix of threshold voltage is computed as a function of top and bottom gate workfunction for determining an optimum value aiming towards competent electrical characteristics. In addition, the sensitivity analysis reveals that the electrical parameters are rarely susceptible to the source doping density, which may considerably solve the limit of dopant solubility in III-V materials. Moreover, HJ-EHBTFT is dramatically unaffected by the variation of gate overlap length and drain voltage, which makes the device have efficient performance in nanoscale regime.

Keywords: Band to Band Tunnelling; Electron-Hole Bilayer Tunnel Field Effect Transistor; Gate Workfunction; Heterojunction; Subthreshold Swing.

How to cite this article

Ahangari Z. Novel attributes of steep-slope staggered type heterojunction p-channel electron-hole bilayer tunnel field effect transistor. *Int. J. Nano Dimens.*, 2019; 10 (4): 391-399.

INTRODUCTION

Continues scaling of conventional metal oxide field effect transistor (MOSFET) has encountered fundamental limitations, better known as short channel effects. One such constraint is related to the switching speed of the device or subthreshold swing (SS) which is the inverse derivative of the drain current with respect to the gate voltage. In conventional MOSFET, due to the drift-diffusion current mechanism, carriers spill over a gate modulated thermal barrier at the source-channel junction and, as a consequence, this value is limited to SS=60mV/dec, at room temperature. Tunnel field effect transistor (TFET) with band to band current mechanism is considered to be a

potential candidate for traditional MOSFET by providing high switching speed [1-4]. Conventional TFET is a gated reversed bias *p-i-n* diode in which horizontal tunneling occurs from the source region into the channel through the gate modulated source-channel depletion region. However, in order to improve the on-state current of TFET, higher tunneling rate of charge carriers should be generated at the source-channel interface. Evidently, increasing the source doping density reduces the space charge region width at the tunneling junction and as a consequence, increases the band to band tunneling rate. New structures and materials such as heterojunction TFETs based on III-V materials are also proposed to boost the

* Corresponding Author Email: z.ahangari@gmail.com

tunneling current [5-8]. Generally, III-V materials suffer from lower solubility of dopants resulting into difficulties for achieving highly doped source region.

Recently, a novel structure of TFET better known as electron-hole bilayer TFET (EHBTFET) is introduced in which the band to band tunneling (BTBT) phenomena occurs along the intrinsic channel and in the vertical direction. In this situation, the tunneling area increases considerably which makes a notable enhancement in the on-state current [9-13]. The p^+-n^+ tunneling junction in this device is created electrically in the intrinsic channel without additional doping. For an n -TFET operation, the bottom gate workfunction and the negative bias of the bottom gate converts the intrinsic bottom layer of the channel to a p^+ accumulated area. Due to the intrinsic region in the top layer of the channel, the depletion barrier width between the top and bottom layer of the channel is not thin enough to allow the carriers to tunnel through vertically. However, as the top gate voltage increases towards sufficient positive values, electrons are accumulated in the top layer and as a consequence, an n^+ region is induced in the top layer channel. Evidently, the formation of p^+-n^+ region in the bottom and top layer of the channel boosts the tunneling rate and band to band tunneling current occurs in the vertical direction. Heterogate configuration is proposed for controlling the excessive tunneling current [14-15], and impact of different channel materials including III-V [16] and germanium [17-18] on the performance of EHBTFET are investigated. The gate leakage current that may effectively deteriorate the device performance is thoroughly investigated in [19] and a gate stack is introduced that can considerably diminish the gate current. New 3D finFET structures are also investigated in which the gates are located at each side of the silicon-based fin and the band to band tunnelling area is created along the fins [20-21]. However, one of the main drawbacks of the proposed electron-hole bilayer TFETs is the employment of opposite biases for the top and bottom gates.

In this paper, the electrical characteristics of a p -channel heterojunction EHBTFET (HJ-EHBTFET) are thoroughly investigated and impact of structural and physical design parameters on the efficient performance of the device is assessed. The performance of heterojunction p -channel device may pave the way for designing low power

steep-slope logic devices. The heterojunction InAs/GaAs_{0.1}Sb_{0.9} has small lattice mismatch and the formation of staggered type interface provides superior electric field to be applied at the tunneling junction that eventually facilitates BTBT current. In addition, the bottom gate bias is totally omitted with the help of appropriate bottom gate workfunction engineering, which facilitates the employment of this device in integrated circuits. Sensitivity analysis of HJ-EHBTFET's main electrical parameters is accomplished via calculating their related standard deviation and mean values to elucidate the variation of proposed device performance with respect to the variation of design parameters. The paper is outlined as follows: the simulation models and proposed device structure are introduced in section two. Following that, the electrical characteristics of HJ-EHBTFET is extensively investigated in section three and finally, the conclusion of the paper is summarized in section four.

EXPERIMENTALS

The schematic of the proposed device is presented in Fig. 1(a), in which HJ-EHBTFET structure consists of InAs n^+ source region, an intrinsic GaAs_{0.1}Sb_{0.9} top channel region, an intrinsic InAs bottom channel region and GaAs_{0.1}Sb_{0.9} p^+ drain region. The top and bottom gate workfunction has different values to facilitate electrical formation of n^+-p^+ junction in the channel. In the on-state mode, depicted in Fig. 1(b), the bottom gate workfunction with zero bias (V_{BG}) induces electrons in the bottom layer of the channel and by applying negative bias to the top gate (V_{TG}), a hole accumulated area is formed in the top layer channel. In this situation, vertical band to band tunneling occurs along the channel thickness. The 2D schematic of conventional TFET is illustrated in Fig. 1(c), with similar bias voltage for the top and bottom gates in which the tunneling barrier is created horizontally from source to channel. In addition, metal gate is considered for the top and bottom gates. Tantalum with workfunction value of 4.8eV is considered for the top gate and chromium with workfunction value of 4.5 eV has been chosen for the bottom gate. It is worth notifying that a framework of metal gate workfunction engineering is conducted to optimize the device performance. The initial device parameters of HJ-EHBTFET and conventional TFET are presented in Table 1. The electrical characteristics of the device

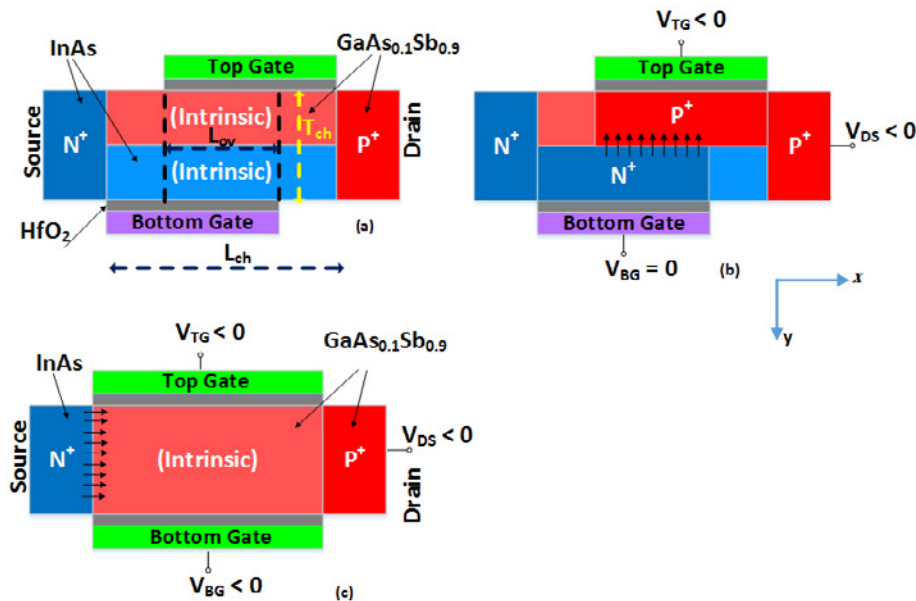


Fig. 1. (a) Schematic of the proposed *p*-channel HJ-EHBTFFET (b) Vertical band to band tunnelling in the on-state operation of HJ-EHBTFFET (c) Conventional TFET operation with horizontal tunnelling direction from source to channel.

Table 1. Initial physical and structural design parameters for the proposed HJ-EHBTFFET and conventional

Parameter	HJ-EHBTFFET	Conventional TFET
Channel length (nm)- L_{ch}	150	150
Gate overlap length (nm)- L_{ov}	50	50
Channel thickness (nm)- T_{ch}	10	10
Top-gate workfunction (eV)	4.8	4.8
Bottom-gate workfunction (eV)	4.5	4.8
Source doping conc. (cm^{-3})	5×10^{18} (n-type)	5×10^{18} (n-type)
Channel doping conc. (cm^{-3})	intrinsic	Intrinsic
Drain doping conc. (cm^{-3})	5×10^{18} (p-type)	5×10^{18} (p-type)
Gate oxide thickness (nm)- HfO_2	1	1

are evaluated via numerical device simulator Silvaco (ATLAS) [22] and following models are considered for analyzing the device:

- Nonlocal band to band tunneling model is employed for considering vertical tunneling of carriers from electrically doped bottom n^+ layer to the p^+ top layer in the channel.
- Recombination models including Shockley–Read–Hall and Auger are considered to calculate the excessive tunneling current results from formation of traps and defects
- In the proposed HJ-EHTFET structure, the carriers are confined along the channel thickness. Obviously, scaling the channel thickness may affect the energy states in the channel. Consequently, quantum confinement model is activated.
- For precise computation of the tunneling current, mobility models including the effect of

doping concentration besides high vertical and lateral electric field are considered.

- Band gap narrowing model is activated for considering the effect of heavily-doped regions on material’s band gap energy.

RESULTS AND DISCUSSIONS

Band to band tunneling mechanism is the main current component of HJ-EHBTFFET and occurs in the channel in which n^+ - p^+ tunneling junctions in the bottom and top layer of the channel are created electrically. The workfunction difference between the bottom gate material and the channel region modulates the electron concentration in the channel in the absence of bottom gate voltage. In addition, a negative voltage is applied to the top gate that accumulates holes in the top layer of the channel region. Similar to conventional TFET, an n^+ - p^+ junction is electrically created in



the intrinsic channel. The carriers in the source diffuse gradually to the bottom layer channel and when sufficient negative bias is applied to the top gate, the potential barrier becomes thin enough and carriers are allowed to tunnel in the vertical direction. The band to band tunnelling energy window ($\Delta\phi$) is described as the energy difference between the minimum value of the bottom layer channel conduction band and maximum of the top layer channel valence band, which is modulated by the top gate voltage. The subthreshold swing in HJ-EHBTFFET is approximately expressed as:

$$SS \approx \frac{\ln(10)}{|q|} \Delta\phi = \frac{\ln(10)}{|q|} (E_c^{\text{bottom-ch}} - E_v^{\text{top-ch}}) \quad (1)$$

Where q , is the electric primitive charge, $E_c^{\text{bottom-ch}}$ is the bottom layer channel conduction band minima and $E_v^{\text{top-ch}}$ denotes the top layer channel valence band maxima, respectively. Clearly, as the top gate bias has increased towards adequate negative values, the approach of $\Delta\phi \rightarrow 0$

provides lower subthreshold swing.

The energy band diagram of HJ-EHBTFFET in the vertical direction and along the channel thickness is presented in Fig. 2(a) in the off-state ($V_{BG}=V_{TG}=0V$) and Fig. 2(b) in the on-state operation ($V_{BG}=0V, V_{TG}=-1V$), while the drain voltage (V_{DS}) is considered $V_{DS}=-0.5V$. Evidently, in the off-state, the wide potential barrier at the interface of the top and bottom channel layers declines the tunneling probability. However, by employing adequate negative top gate voltage, the negative potential in the top layer of the channel is increased and when the conduction band of the bottom layer channel is moved below the valence band of the channel top layer, BTBT is strongly enhanced. Obviously, as the current transport of the proposed HJ-EHBTFFET depends upon quantum tunneling and does not suffer from thermionic emission, a fast switching speed with small SS can be achieved.

The electron and hole concentration of the channel are calculated in the off-state and on-state along the channel thickness, Fig. 3. In

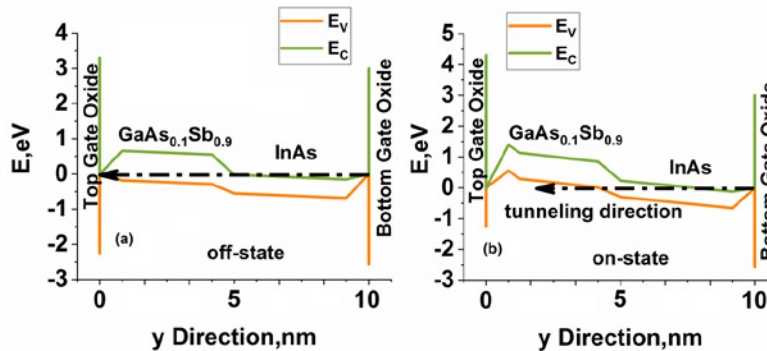


Fig. 2. Energy band diagram along the channel thickness in the (a) off-state and (b) on-state operation. The arrow shows the tunnelling barrier width.

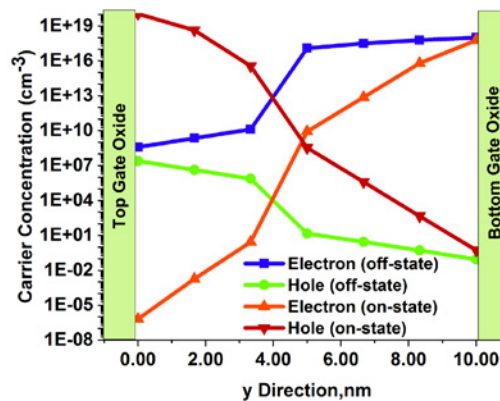


Fig. 3. Electron and hole concentration along the channel thickness from top gate to the bottom gate in the off-state and on-state operation.

the off-state, the electron concentration in the bottom layer channel is considerably increased due to the bottom gate workfunction coupling over the channel, while as moving to the top layer of the channel, the region keeps its intrinsic characteristics. However, by increasing the negative top gate bias, the intrinsic region is converted to a hole accumulated area.

Top and bottom gate workfunction are critical design parameters that considerably affect the induced electron and hole concentration in the channel and as a consequence, affect the tunneling probability. The transfer characteristics of HJ-EHBTFT are illustrated in Fig. 4 as the top gate workfunction is varied. The threshold voltage (V_{th}) is defined as the gate voltage value in which the drain current transits from the off-state to on-state. Due to the increment of workfunction difference between the top gate workfunction

and the channel material, the induced hole concentration in the top layer of the channel increases considerably. Accordingly, the threshold voltage of the device decreases as the top gate workfunction approaches to 5eV. A step-like behavior is observed in the transfer characteristics and for WFT=4.8eV with low negative threshold voltage, on/off current ratio of 3.85×10^{13} and subthreshold swing of $SS=2mV/dec$ are achieved. On the other hand, bottom gate workfunction is responsible for modulating the n^+ bottom layer that will dramatically affect the tunneling barrier width in the vertical direction. The transfer characteristics of HJ-EHBTFT are depicted in Fig. 5, as the bottom gate workfunction is parameterized. Clearly, as the bottom gate workfunction is reduced, the increment of accumulated electrons in the bottom layer reduces the tunneling barrier width and as a consequence, higher electric field is

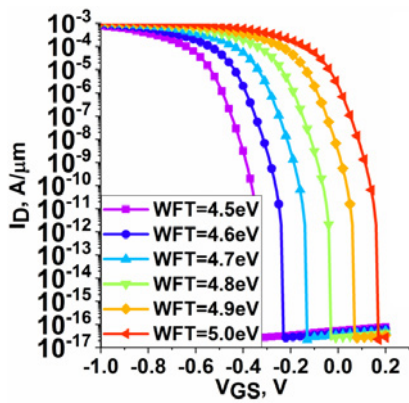


Fig. 4. Transfer characteristics of HJ-EHBTFT for $V_{DS}=-0.5V$. Top gate workfunction is parameterized, while the bottom gate workfunction is constant at WFB=4.8eV.

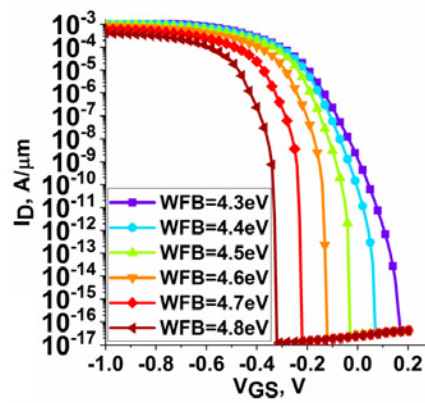


Fig. 5. I_D-V_{GS} curve of HJ-EHBTFT for $V_{DS}=-0.5V$ while the bottom gate workfunction is varied, considering the top gate workfunction constant at WFT=4.5eV.

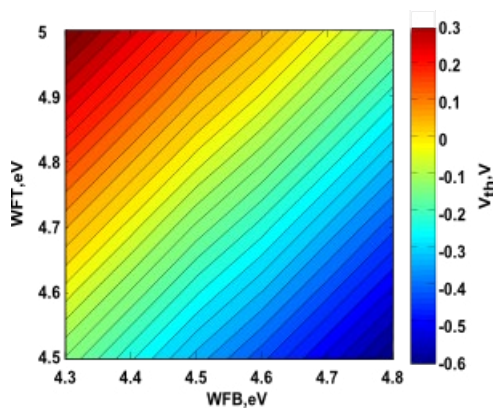


Fig. 6. 2D contour of V_{th} variation as a function of top and bottom gate workfunction.

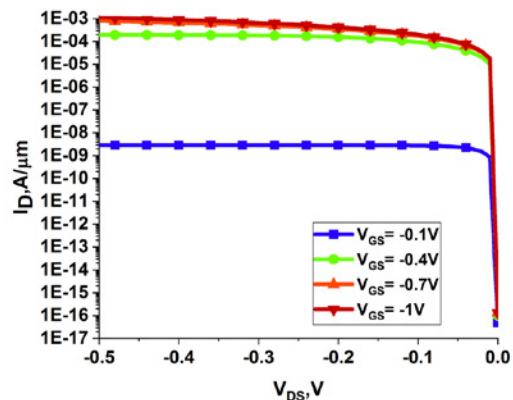


Fig. 7. Output characteristics of HJ-EHBTFT as a function of top gate voltage.

induced that assists the on-state current.

The transition voltage from off-state to on-state considerably depends upon the threshold voltage and as result, determining the optimum value for the top gate and bottom gate workfunction providing high on/off current ratio, lowest possible negative threshold voltage value beside steep subthreshold swing, is critical. The two dimensional (2D) variation matrix of the threshold voltage is computed as a function of top and bottom gate workfunction, depicted in Fig. 6. Maximum negative threshold voltage is obtained at the bottom right corner of the variation matrix where high workfunction value of the bottom gate reduces the induced electron concentration in the bottom layer channel and as a consequence, leads to the increment of the tunneling barrier width. On the other hand, maximum positive voltage that result in the increment of the off-state current (at $V_{TG}=0V$) is obtained on the top left corner of the variation contour. This is due to the fact that for low workfunction values of the bottom gate, the density of accumulated electron is increased in the bottom layer and besides that, due to enhanced value of top gate workfunction, the density of holes increases considerably. In this situation, the tunneling window becomes narrow enough for sufficient carrier tunneling.

The output characteristics ($\log(I_D)-V_{DS}$) of HJ-EHBTFT are illustrated in Fig. 7. The top gate voltage variation has a great impact on the drain current and when the gate voltage exceeds beyond the threshold voltage from $V_{GS} = -0.1V$, a sharp increase in the current is observed and

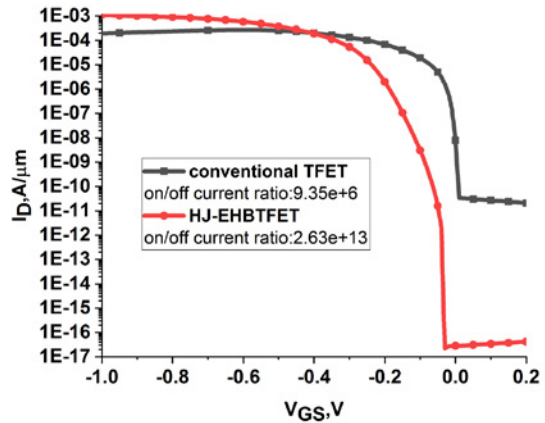


Fig. 8. I_D-V_{GS} curve of conventional TFET and HJ-EHBTFT for $V_{DS} = -0.5 V$.

demonstrates that the abrupt transition from off to on state is the main feature of the proposed device.

The electrical characteristic of conventional TFET ($WFT=WFB=4.8eV$) is computed and the results are compared with the transfer characteristic of HJ-EHBTFT, depicted in Fig. 8. Due to the electrically formation of tunneling junction along the channel thickness, the drain voltage is mainly limited at the drain side and as a result, a sufficiently large tunneling barrier is created in the off-state mode of HJ-EHBTFT. This feature of increasing the off-state tunneling barrier width besides the increment of vertical tunneling area that leads to the excessive on-state current, provides remarkable improvement of on/off current ratio in comparison with the

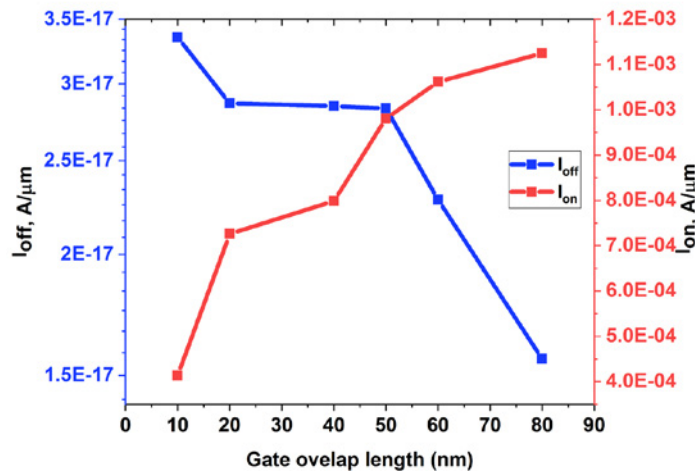


Fig. 9. Off-state and on-state current of HJ-EHBTFT as a function of gate overlap region.

conventional TFET. However, in the conventional TFET, band to band tunnelling mainly occurs within a limited area at the source channel interface that eventually makes the on-state current reduce in comparison with bilayer TFET. It is worth notifying that due to the top and bottom gate asymmetric location, different gate workfunction values and the bilayer heterojunction channel, the proposed device requires complex fabrication process in comparison with conventional TFET. However, the vertical fabrication process of double-gate TFET employing MBE growth can be considered as an approach for fabricating the proposed device [23].

The effect of gate scaling on the performance of HJ-EHBTFTFET is considered while the gate overlap region is varied from $L_{ov}=10\text{nm}$ to $L_{ov}=80\text{nm}$, depicted in Fig. 9. The reduction of gate overlap region would slightly reduce the 2D tunnelling area ($L_{ov} \times$ lateral width of the device). However, the main feature of this device is the insensitivity of the off-state current (I_{off}) and subthreshold swing to the reduction of gate length that facilitates the scaling of this device towards nanoscale regime.

The effect of drain bias on the performance of HJ-EHBTFTFET is accessed via simulating the transfer characteristics of the device as the drain voltage is parameterized, depicted in Fig.10. Clearly, the increment of the drain bias enhances the carrier velocity and as a consequence leads to the amplification of the on-state current. However, the main feature of the proposed device is the low susceptibility of the off-state current to the drain voltage, implicating the immunity of device to short channel effects. The ultra-thin body double-gate structure that is considered in this study, in which the carrier transport is quantized in one direction, can be considered as a square potential well. Due to the size quantization, the band gap energy of ultra-thin-body structures increases from the bulk value [24-25]. In this situation, the critical peak electric field can be effectively enhanced. This effect is more pronounced in III-V

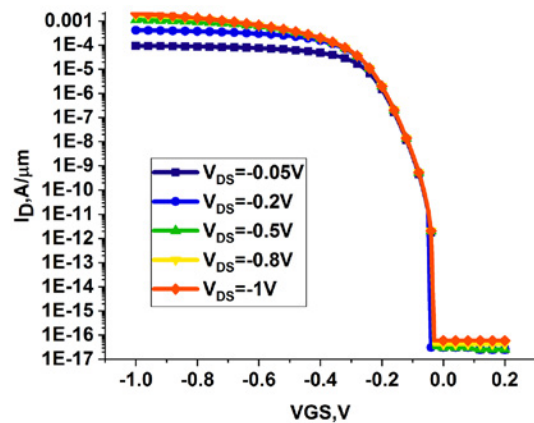


Fig. 10. I_D - V_{GS} curve of HJ-EHBTFTFET as a function of drain bias.

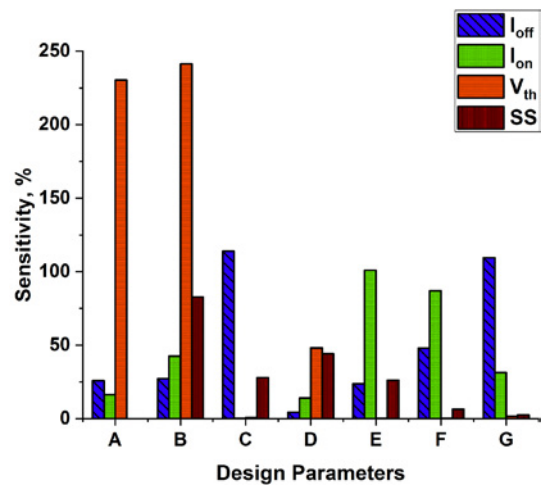


Fig. 11. Sensitivity of main electrical parameters with respect to the variation of physical and structural design parameters. A: Top gate workfunction, B: Bottom gate workfunction, C: Source doping density, D: Channel thickness, E: Gate overlap length, F: Drain voltage and G: Drain doping.

materials employing low effective mass for the carriers. The band gap of bulk InAs is 0.34eV and the critical electric field is $4 \times 10^4 \text{ V/cm}^{-1}$. However, the calculated peak electric field in our simulation

Table 2. Standard deviation (sigma) and mean value of main electrical parameters for HJ-EHBTFTFET.

Electrical Parameters	$I_{on}(\text{mA}/\mu\text{m})$		$I_{off}(\text{A}/\mu\text{m}) \times 10^{-16}$		$ V_{th} (\text{V})$		SS(mV/dec)	
	sigma	mean	sigma	mean	sigma	mean	sigma	mean
WFT (4.5: 5.1eV)	0.167	1.03	0.09	0.37	0.19	0.081	0	2
WFB (4.3: 4.8eV)	0.4	0.95	0.084	0.31	0.18	0.075	2.80	3.39
Source Dop. Conc. (10^{18} : 10^{20} cm^{-3})	0.003	1.12	0.75	0.66	0.0	0.03	0.65	2.33
V_{DS} (-0.05: -1 V)	0.81	1.06	0.038	0.29	0	0.03	0.13	2.02
L_{ov} (10: 80 nm)	0.26	0.85	0.06	0.26	0.0	0.03	0.61	2.35
Channel thickness (5: 15nm)	0.12	0.9	0.01	0.28	0.01	0.031	1.1	2.49
Drain Dop. Conc. ($10^{18.5}$: 10^{19} cm^{-3})	0.38	1.21	0.3	0.27	0.0005	0.029	0.05	2.03



study is 1×10^6 V/cm¹. The band gap energy of 5nm 2D InAs channel is 0.75eV [25] and for GaAs_{0.1}Sb_{0.9}=1.1eV.

Next, the sensitivity of device main electrical parameters with respect to the variation of physical and structural design parameters is calculated to assess the feasibility of proposed device in nanoscale regime. In the first step, all design parameters are set to their initial values and just one design parameter is varied. Following that, main electrical parameters including off-state current, on-state current, V_{th} and SS are calculated. In the last step, mean and standard deviation values of each electrical parameter are calculated, presented in Table 2, and the sensitivity, which is defined as the standard deviation over mean value in percentile, is computed and illustrated in Fig. 11. The top and bottom gate workfunction considerably affect the bias induced charge carriers along the channel thickness and as a consequence, modulate the tunneling barrier. It is expected that the threshold voltage of the device is highly sensitive to the gate workfunction variation. Evidently, in conventional TFET, highly doped source region makes an abrupt source-channel tunnelling barrier that facilitates the tunnelling rate. However, one of the main limitations of III-V materials is the low solubility of dopants which constrains highly doped source and drain regions. The on-state sensitivity profile reveals that, in HJ-EHBTFT, the electrical parameters are rarely susceptible to the variation of source doping density, which facilitates fabrication of the device for nanoscale applications. In addition, the off-state current and subthreshold swing are not affected by the variation of gate overlap length and drain voltage which shows high immunity of the proposed device to short channel effects.

CONCLUSION

In conclusion, a new p-channel device architecture better known as heterojunction electron-hole bilayer tunnel field effect transistor is thoroughly investigated. The tunneling n⁺-p⁺ junction is electrically created in the intrinsic channel and in the vertical direction, which can considerably improve the on-state current. The workfunction difference between gate material and the channel region modulates the induced carrier density in the channel and as a consequence, affects the tunneling barrier width. Obviously, optimized value should be determined

for the top and bottom gate workfunction. Next, sigma over mean value in percentile of main electrical parameters demonstrates that the device is less sensitive to the variation of source doping density, channel length and drain voltage, which makes the device a potential candidate for digital applications in nanoscale regime.

CONFLICT OF INTEREST

The authors declare that they have no competing interests.

REFERENCES

1. Lin Y. K., Khandelwal S., Duarte J. P., Chang H. L., Salahuddin S., Hu C., (2017), A predictive tunnel FET compact model with atomistic simulation validation. *IEEE Transact. Elect. Dev.* 64: 599-605.
2. Ahangari Z., (2018), Performance investigation of a semi-junctionless type II heterojunction tunnel field effect transistor in nanoscale regime. *Micro & Nano Lett.* 13: 1165-1169.
3. Boucart K., Ionescu A. M., (2007), Double-gate tunnel FET with high- κ gate dielectric. *IEEE Transact. Elect. Devic.* 54: 1725-1733.
4. Khorramrouz F., Sedigh Ziabari S. A., Heydari A., (2018), Analysis and study of geometrical variability on the performance of junctionless tunneling field effect transistors: Advantage or deficiency?. *Int. J. Nano Dimens.* 9: 260-272.
5. Hanna A. N., Fahad H. M., Hussain M. M., (2015), InAs/Si hetero-junction nanotube tunnel transistors. *Scientific Rep.* 5: 9843-9847.
6. Wang Y., Liu Y., Han G., Wang H., Zhang C., Zhang J., Hao Y., (2017), Theoretical investigation of GaAsBi/GaAsN tunneling field-effect transistors with type-II staggered tunneling junction. *Superlatt. Microstruc.* 106: 139-146.
7. Shih P. C., Hou W. C., Li J. Y., (2017), A U-gate InGaAs/GaAsSb heterojunction TFET of tunneling normal to the gate with separate control over ON-and OFF-state current. *IEEE Elect. Dev. Lett.* 38: 1751-1754.
8. Pown M., Lakshmi B., (2017), Performance analysis of InAs-and GaSb-InAs-based independent gate tunnel field effect transistor RF mixers. *J. Comput. Elect.* 16: 676-684.
9. Lattanzio L., De Michielis L., Ionescu A. M., (2011), Electron-hole bilayer tunnel FET for steep subthreshold swing and improved ON current. In *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)* (pp. 259-262). IEEE.
10. Alper C., Palestri P., Padilla J. L., Ionescu A. M., (2016), The electron-hole bilayer TFET: Dimensionality effects and optimization. *IEEE Transac. Elect. Dev.* 63: 2603-2609.
11. Lattanzio L., De Michielis L., Ionescu A. M., (2012), The electron-hole bilayer tunnel FET. *Solid-State Electron.* 74: 85-90.
12. Revelant A., Villalon A., Wu Y., Zaslavsky A., Le Royer C., Iwai H., Cristoloveanu S., (2014), Electron-hole bilayer TFET: Experiments and comments. *IEEE Transac. Elect. Dev.* 61: 2674-2681.
13. Loan S. A., Alharbi A. G., Rafat M., (2018), Ambipolar leakage suppression in electron-hole bilayer TFET: Investigation and

- analysis. *J. Comput. Electron.* 17: 977-985.
14. Padilla J. L., Alper C., Gamiz F., Ionescu A. M., (2016), Switching behavior constraint in the heterogate electron-hole bilayer tunnel FET: The combined interplay between quantum confinement effects and asymmetric configurations. *IEEE Transact. Elect. Dev.* 63: 2570-2576.
 15. Padilla J. L., Alper C., Gámiz F., Ionescu A. M., (2014), Assessment of field-induced quantum confinement in heterogate germanium electron-hole bilayer tunnel field-effect transistor. *Appl. Phys. Lett.* 105: 082108-082112.
 16. Kim S. Y., Seo J. H., Yoon Y. J., Lee H. Y., Lee S. M., Cho S., Kang I. M., (2015), Design and analysis of CMOS-compatible III-V compound electron-hole bilayer tunneling field-effect transistor for ultra-low-power applications. *J. Nanosci. Nanotechnol.* 15: 7486-7492.
 17. Jeong W. J., Kim T. K., Moon J. M., Park M. G., Yoon Y. G., Hwang B. W., Lee S. H., (2015), Germanium electron-hole bilayer tunnel field-effect transistors with a symmetrically arranged double gate. *Semicond. Sci. Technol.* 30: 035021-035026.
 18. Alper C., Lattanzio L., De Michielis L., Palestri P., Selmi L., Ionescu A. M., (2013), Quantum mechanical study of the germanium electron-hole bilayer tunnel FET. *IEEE Transact. Elect. Dev.* 60: 2754-2760.
 19. Padilla J. L., Medina-Bailon C., Marquez C., Sampedro C., Donetti L., Gamiz F., Ionescu A. M., (2018), Gate leakage tunneling impact on the InAs/GaSb heterojunction electron-hole bilayer tunneling field-effect transistor. *IEEE Transac. Elect. Dev.* 99: 1-8.
 20. Kim S., Choi W. Y., Park B. G., (2018), Vertical-structured electron-hole bilayer tunnel field-effect transistor for extremely low-power operation with high scalability. *IEEE Transac. Elect. Dev.* 65: 2010-2015.
 21. Zhu Z., Zhu H., Xu M., Zhong J., Zhao C., Chen D., Ye T., (2014), A novel fin electron-hole bilayer tunnel field-effect transistor. *IEEE Transact. Nanotech.* 13: 1133-1137.
 22. ATLAS User Manual, Santa Clara, USA: Silvaco International, 2015.
 23. Tura A., Zhang Z., Liu P., Xie Y. H., Woo J. C., (2011), Vertical silicon pnnp tunnel nMOSFET with MBE-grown tunneling junction. *IEEE Transact. Elect. Devic.* 58: 1907-1913.
 24. Ahangari Z., Fathipour M., (2013), Tight-binding study of quantum transport in nanoscale GaAs Schottky MOSFET. *Chinese Phys. B.* 22: 098502-098506.
 25. Ahangari Z., (2016), Impact of Indium mole fraction on the quantum transport of ultra-scaled In_xGa_{1-x}As double-gate Schottky MOSFET: Tight-binding approach. *Appl. Phys. A.* 122: 69-75.