Int. J. Nano Dimens., 10 (4): 368-374, Autumn 2019

ORIGINAL ARTICLE

Improved drain current characteristics of tunnel field effect transistor with heterodielectric stacked structure

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Received 01 June 2019; revised 17 July 2019; accepted 23 July 2019; available online 30 July 2019

Abstract

In this paper, we proposed a 2-D analytical model for electrical characteristics such as surface potential, electric field and drain current of Silicon-on-Insulator Tunnel Field Effect Transistor (SOI TFETs) with a SiO_2/High-k stacked gate-oxide structure. By using superposition principle with suitable boundary conditions, the Poisson's equation has been solved to model the channel region potential. The modeled channel potential is to calculate both vertical and lateral electric field. 2-D Kane's model is used to calculate the drain current of TFET and the expression is taken out by analytically integrating the band-to-band tunneling generation rate over the thickness of channel region. The device is modeled in variation with different device parameters like channel length (L_{CH}), dielectric thickness (t_{ox}), silicon thickness (t_{si}) and input voltage (V_{ds} and V_{gs}). Also, the comparison of SiO_2 and stacked high k dielectric TFET is obtained. It has been found from the presented results that the hetero-dielectric stacked TFET structure provides ON current 10^{-6}A/um. However, SiO_2 dielectric structure provides the ON current of 10^{-8}A/um. The proposed model is validated by comparing it with Technology Computer-Aided Design (TCAD) simulation results obtained by using SILVACO ATLAS device simulation software.

Keywords: *Analytical Modeling; High-k Dielectric; Poisson's Equation; Superposition Principle; Tunnel FET (TFET).*

How to cite this article

Palanichamy V, Kulkarni N, Thankamony Sarasam AR. Improved drain current characteristics of tunnel field effect transistor with heterodielectric stacked structure. Int. J. Nano Dimens., 2019; 10 (4): 368-374.

INTRODUCTION

In this era of modern VLSI industry, power efficient and economical semiconductor devices play a major role in the semiconductor market. To cater this and improve efficiency of the device, the dimensions of the Metal oxide semiconductor field effect transistors (MOSFETs) are being continuously scaled down in nano meter range [1-4], resulting in accretion of few performance limitations called as Short Channel Effects (SCE). By using various novel devices like impact-ionization MOS devices [5-7], Nano-Electro Mechanical FETs (NMFETs), Suspended Gate MOSFETs, Multi Gate MOSFETs, Silicon on Insulator Field Effect Transistors (SOI FETs), Fin FETs, etc., these effects are overwhelmed. Yet power efficiency being the major issue in these novel devices, Since an assuring device structure is modelled to improve power efficiency termed as Tunnel Field Effect Transistors (TFETs) [8, 9]. This is a better replacement for MOSFETs because of its low and steeper sub threshold swing (SS) less than 60 mV/dec (SS for conventional MOSFETs limited to 60 mV/decade). In order to improve the ON current [10-14] of these devices high-k materials are stacked with SiO_2 in gate dielectric region, by this electrical characteristic of the TFETs are improved.

In this paper, a 2-D analytical solution of SOI TFETs with a SiO_2/High-k stacked gate-oxide structure has been presented. A two-dimensional Poisson's equation has been solved to derive the analytical expressions for surface potential and electrical field. By varying the surface potential, the electric field is obtained and is used for deriving the drain current by applying Kane's model [15] for tunnelling. This paper is presented as follows: The device structure of high-k stacked gate oxide TFET is explained in the section II. The adaption of 2-D

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Poisson's equation and Kane's model in finding analytical solutions for surface potential, electric field and drain current in the channel respectively are derived in the section III. In Section IV the model is validated by comparing it with TCAD 2D simulation results for various parameters like channel length, dielectric thickness (t_{ox}) and thickness of layer (t_{si}) with different voltages. The I_{DS} –V_{gs} characteristics are obtained by using BTBT rate generation (G).

MATERIALS AND METHODS

Device Structure

The cross-sectional view of SOI TFET with high-k SiO_2/HfO_2 stacked gate-oxide structure is shown in Fig. 1, where t_{SiO2} is the thickness of gate oxide, t_k is the thickness of high-k material, t_{ox} is thickness of stacked gate dielectric, t_{si} is the silicon thickness, L_{CH} is the length of the channel device and t_{BOX} is the thickness of bottom of the buried oxide layer which should be grounded. If the thickness of BOX layer (t_{BOX}) is excessively small; then voltage drop across BOX region will be negligible. The X-axis is represented along the channel length and Y- axis has been considered along channel oxide thickness.

Table 1 shows the materials and parameters used for the proposed device structure and its dimensions also.

To study the device physics and to analyse the device characteristics the mathematical methods are included for the proposed device structure as given in this section. The surface potential in the channel and gate oxide region of TFET is given by 2 dimensional Poisson's equation:

$$\frac{\partial^2 \varphi}{\partial x^2} + \frac{\partial^2 \varphi}{\partial y^2} = 0 \quad (1)$$

By solving (1), here it is assumed that the gate oxide region is replaced by silicon material which is considered as permittivity difference. Hence, the thickness of oxide (t_{SiO_2}) is converted by t_{1ox} which is given as,

$$t_{1ox} = \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{SiO_2} \quad (2)$$

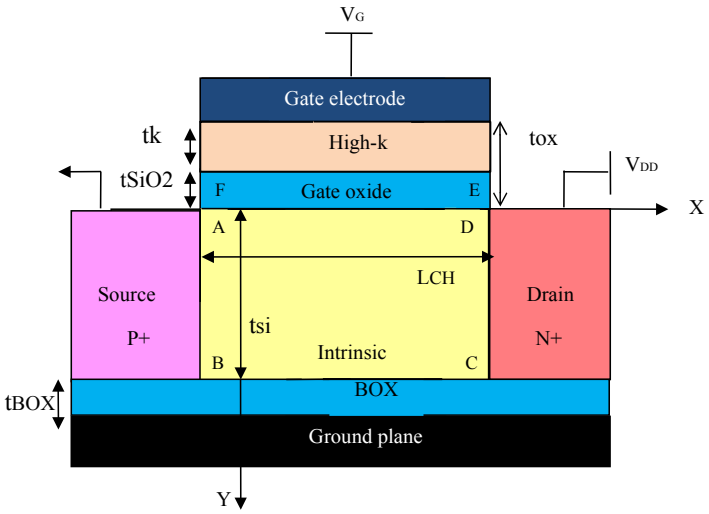

Fig. 1. Cross-sectional view of SOI TFET with high-k SiO_2/HfO_2 stacked gate-oxide.

Table.1. Device Dimensions for SOI TFET with high-k SiO_2/HfO_2 stacked gate-oxide.

Sl. No.	Parameter	Variable	Dimensions
1	Channel Length	L_{Ch}	30 nm
2	Silicon Thickness	t_{Si}	10 nm
3	Thickness of Silicon Dioxide	t_{SiO2}	2 nm
4	Thickness of High-k Dielectric (H_{fO2})	t_{hk}	1 nm
5	Thickness of Buried Oxide	t_{box}	20 nm
6	Source Doping Concentration	p+	10^{20} cm^3
7	Channel Doping Concentration	n	10^{20} cm^3
8	Drain Doping Concentration	n+	10^{16} cm^3

where ε_{si} - relative permittivity of silicon and ε_{ox} - relative permittivity of silicon dioxide.

To improve the device performance along with SiO_2 high-k dielectric is also stacked. It is noted that the high-k dielectric of thickness t_k can be considered as an equivalent SiO_2 thickness ($\varepsilon_{ox} t_k / \varepsilon_k$) and hence the stacked gate dielectric structure can be ascertained to be a single SiO_2 layer. The thickness of stacked gate dielectric structure is given as,

$$t_{ox} = t_{SiO_2} + \varepsilon_{ox} t_k / \varepsilon_k \tag{3}$$

By considering (3), we can modify (2) for stacked gate dielectric structure as,

$$t_{1oxk} = \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} \tag{4}$$

The boundary conditions for channel region:

$$\varphi(0, y) = -\varphi_{bi} = -\frac{E_g}{2q} = \varphi_{AB} \tag{5}$$

$$\varphi(L_{ch}, y) = \varphi_{bi} + V_{ds} = \varphi_{CD} \tag{6}$$

$$\varphi(x, t_{si}) = 0 = \varphi_{BC} \tag{7}$$

The boundary conditions for gate oxide region:

$$\varphi(x, -t_{1oxk}) = V_{gs} - V_{fb} = \varphi_{FE} \tag{8}$$

$$\varphi(0, y) = \frac{\varphi_{AB} - \varphi_{FE}}{t_{1oxk}} y + \varphi_{AB} = \varphi_{FA} \tag{9}$$

where, V_{gs} is the gate voltage, V_{fb} is the flat band voltage, φ_{bi} is built in potential, q is the elementary charge and E_g is the band gap energy.

The general solution of (1) is written as,

$$\varphi(x, y) = V(y) + u_L(x, y) + u_R(x, y) \tag{10}$$

where, $u_L(x, y)$ and $u_R(x, y)$ are the solution of (1).

V(y) is the solution of one-dimensional Poisson's equation in Y-direction as follows:

$$V(y) = -\frac{\varphi_s}{t_{si}}(y - t_{si}) \quad \text{in the channel region} \tag{11}$$

$$V(y) = \frac{\varphi_s - \varphi_{FE}}{t_{1oxk}} y + \varphi_s \quad \text{in the gate oxide region} \tag{12}$$

where φ_s is the surface potential ,which is given as,

$$\varphi_s = \frac{V_{gs} - V_{fb}}{1 + t_{10xk} / t_{si}} \tag{13}$$

By separation of variables, $u_L(x, y)$ and $u_R(x, y)$ can be rewritten as follows:

$$u_L(x, y) = \sum_{n=1}^{\infty} b^*_n \frac{\sinh\left(\frac{n\pi(L_{CH} - x)}{\beta}\right)}{\sinh\left(\frac{n\pi L_{CH}}{\beta}\right)} \sin\left(\frac{n\pi(y + t_{1oxk})}{\beta}\right) \tag{14}$$

$$u_R(x, y) = \sum_{n=1}^{\infty} c^*_n \frac{\sinh\left(\frac{n\pi x}{\beta}\right)}{\sinh\left(\frac{n\pi L_{CH}}{\beta}\right)} \sin\left(\frac{n\pi(y + t_{1oxk})}{\beta}\right) \tag{15}$$

where $\beta = t_{si} + t_{1oxk}$

The co-efficient b^*_n and c^*_n values has been taken from [15]. Hence (10) can be rewritten as,

$$\varphi(x, y) = \left\{ \begin{array}{l} -\frac{\varphi_s}{t_{si}}(y - t_{si}) + \sum_{n=1}^{\infty} b^*_n \frac{\sinh\left(\frac{n\pi(L_{CH} - x)}{\beta}\right)}{\sinh\left(\frac{n\pi L_{CH}}{\beta}\right)} \sin\left(\frac{n\pi(y + t_{1oxk})}{\beta}\right) \\ + \sum_{n=1}^{\infty} c^*_n \frac{\sinh\left(\frac{n\pi x}{\beta}\right)}{\sinh\left(\frac{n\pi L_{CH}}{\beta}\right)} \sin\left(\frac{n\pi(y + t_{1oxk})}{\beta}\right) \end{array} \right\}$$

in the channel region (16)

$$\varphi(x, y) = \left\{ \begin{array}{l} \frac{\varphi_s - \varphi_{FE}}{t_{1ox}} y + \varphi_s + \sum_{n=1}^{\infty} b^*_n \frac{\sinh\left(\frac{n\pi(L_{CH} - x)}{\beta}\right)}{\sinh\left(\frac{n\pi L_{CH}}{\beta}\right)} \sin\left(\frac{n\pi(y + t_{1oxk})}{\beta}\right) \\ + \sum_{n=1}^{\infty} c^*_n \frac{\sinh\left(\frac{n\pi x}{\beta}\right)}{\sinh\left(\frac{n\pi L_{CH}}{\beta}\right)} \sin\left(\frac{n\pi(y + t_{1oxk})}{\beta}\right) \end{array} \right\}$$

in the gate oxide region (17)

The total electric field (E) is given as,

$$E = \sqrt{E_x^{\,2} + E_y^{\,2}} \tag{18}$$

where, $E_x(x, y)$ is the lateral electric field of channel and $E_y(x, y)$ is the vertical electric field of channel is obtained from (16).

$$E_x(x, y) = -\frac{\partial \varphi(x, y)}{\partial x} = \sum_{n=1}^{\infty} \frac{n\pi}{\beta} \frac{\sin\left(\frac{n\pi(y + t_{1oxk})}{\beta}\right)}{\sinh\left(\frac{n\pi(L_{CH} - x)}{\beta}\right)} * \left[\begin{array}{l} b^*_n \cosh\left(\frac{n\pi(L_{CH} - x)}{\beta}\right) \\ -c^*_n \cosh\left(\frac{n\pi x}{\beta}\right) \end{array} \right] \tag{19}$$

$$E_y(x,y) = -\frac{\partial\varphi(x,y)}{\partial y} \tag{20}$$

$$= \frac{\varphi_s}{t_{si}} - \sum_{n=1}^{\infty} \frac{n\pi}{\beta} \frac{\cos\left(\frac{n\pi(y - t_{loxk})}{\beta}\right)}{\sinh\left(\frac{n\pi(L_{CH} - x}{\beta}\right)} * \left[b^*_n \sinh\left(\frac{n\pi(L_{CH} - x}{\beta}\right) - c^*_n \sinh h\left(\frac{n\pi x}{\beta}\right) \right]$$

Now the analytical expression of the drain current (I_{DS}) is calculated by integration of BTBT generation rate (G) over channel region. The drain current (I_{DS}) can be expressed as,

$$I_{DS} = q\int G dx dy \tag{21}$$

Kane's model [16] has been employed for the calculating the BTBT generation rate (G)

$$G(E) = A.E \exp\left(\frac{-B}{E}\right) \tag{22}$$

where A and B are the two tunneling process-dependent parameter, their values has been given as 8.1×10^{17} $cm^{-1}s^{-1}V^{-2}$ and 3.057×10^{7}V/cm. E is the total electric field is obtained from (17).

RESULTS AND DISCUSSION

The performance of derived analytical model has been verified and analysed by Technology Computer-Aided Design (TCAD) 2D simulator. The surface potential and electric field are calculated from 2D Poisson's equations. With the variation in channel length (L_{CH}) and voltages (V_{gs} and V_{ds}), the surface potential and electric field graphs are plotted.

Fig. 2 shows the plot of surface potential against the channel location. The surface potential varies with respect to gate voltage V_{gs} (0V to 0.5V) with a constant drain voltage V_{ds} (0.1V) and also the thickness of stacked gate oxide (t_{ox}) and silicon thickness(t_{si}) is 3nm and 50nm respectively. The channel length is kept as 30nm, the gate voltage is varied and the surface potential is varied accordingly. With the increase in the input gate voltage, the surface potential is also increased. Therefore the surface potential linearly increases in the short channel TFETs compared to long channel TFETs. Thus the drain potential affects the entire channel region less in the long channel TFETs than the short channel TFETs. Fig. 3 shows the plots for total electric field E along the channel location with the variation in input gate voltage (say 0.2V, 0.4V and 0.6V). Based on increment in the channel location, E linearly decreases. After a particular point, in the drain region along with E values are linearly increases. It is clearly observed that with the increase in input gate voltage, the total electric field also increases. Thus, the total electric field is directly dependent on the input gate voltage.

The reduction of gate oxide thickness is usually employed to improve the ON-current (I_{ON}) and to attain high ON to OFF current ratios (ION/IOFF) in TFETs. By the derived analytical model for drain current (18), transfer characteristic (IDS –Vgs

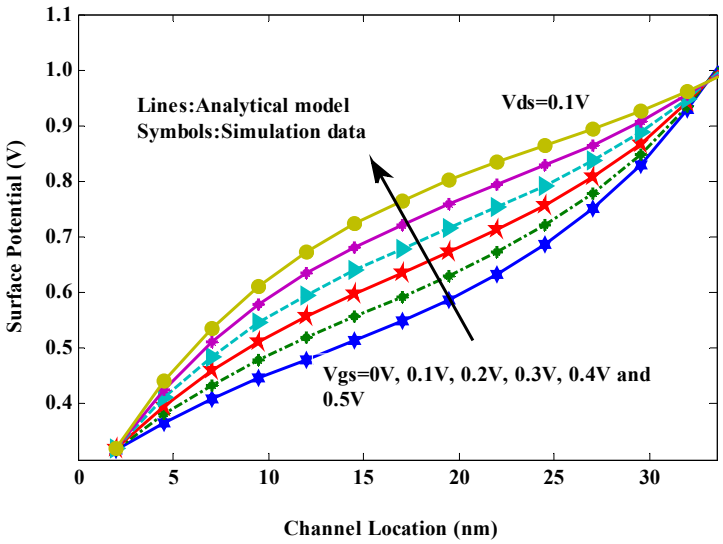

Fig. 2. Surface Potential against channel location in variation with input gate to source Voltage.

characteristics) is plotted in Fig. 4 in logarithmic scale. The plot shows drain current (IDS) along the applied input gate voltage (Vgs) in variation with different dielectric thickness 1 nm, 2 nm & 3 nm respectively. It is clearly observed that for the reduced dielectric thickness (1 nm) shows a better ON current.

Fig. 5, Fig. 6 and Fig. 7 represents the stacked high k (SiO_2/HfO_2) TFET structure is compared with the SOI of SiO_2 gate oxide TFET structure. Fig. 5 shows the plot of surface potential versus channel location. Here channel length kept as 30 nm and voltages V_{ds} and V_{gs} are kept as constant values 0.1V and 0.2V respectively. At certain point, stacked high k of surface potential has better improvement in the surface potential than the SiO_2 structure. Thus stacked high k shows better increment in the surface potential.

A plot of electric field (E) against channel location is shown in Fig. 6. The channel length is 30nm.As compered to SiO_2 structure,the stacked high k TFET of electric field are gradually gets decreased and at certain point, it gradually gets incresed in the drain region. Fig. 7 represent the drain current versus gate voltage, where the thickness of oxide t_{ox} is kept constant as 1nm. As smaller the thickness of oxide, better ON current is achieved. By comparing SiO_2 gate oxide and the stacked high k TFET,stacked high k is producing more drain current.

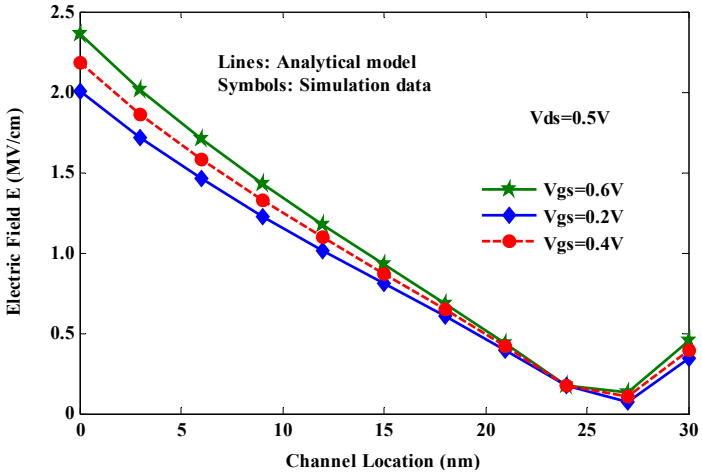

Fig. 3. Total Electric Filed along the channel location in variation with input gate to source Voltage.

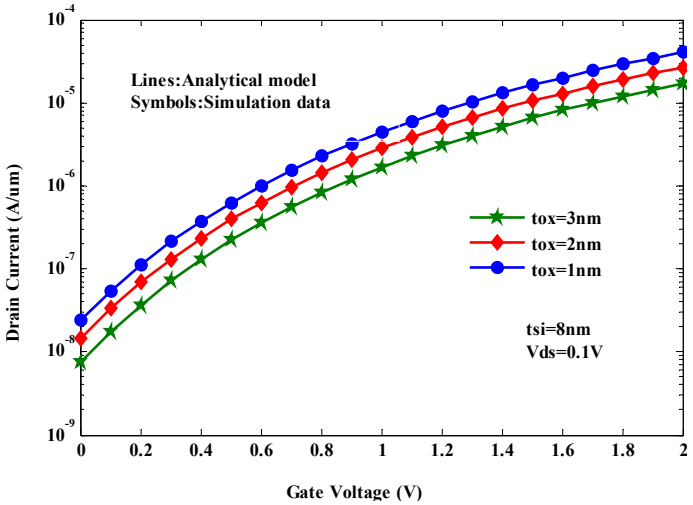

Fig. 4. Transfer characteristics in logarithmic scale in variation with oxide thickness.

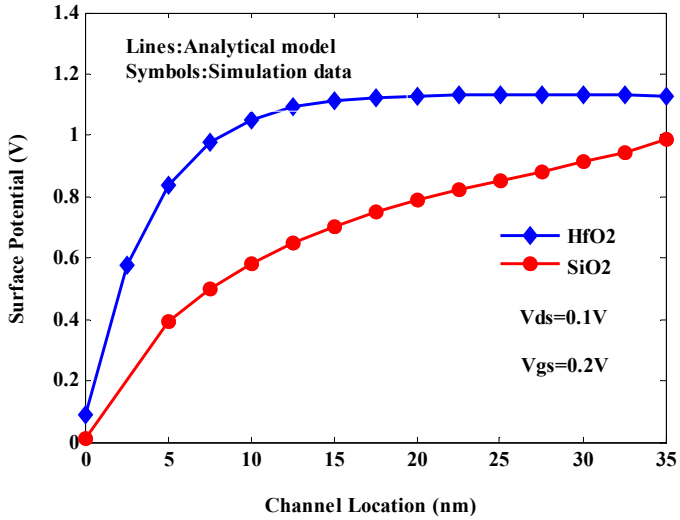

Fig. 5. Surface Potential along the channel location for stacked high-k dielectric and SiO_2.

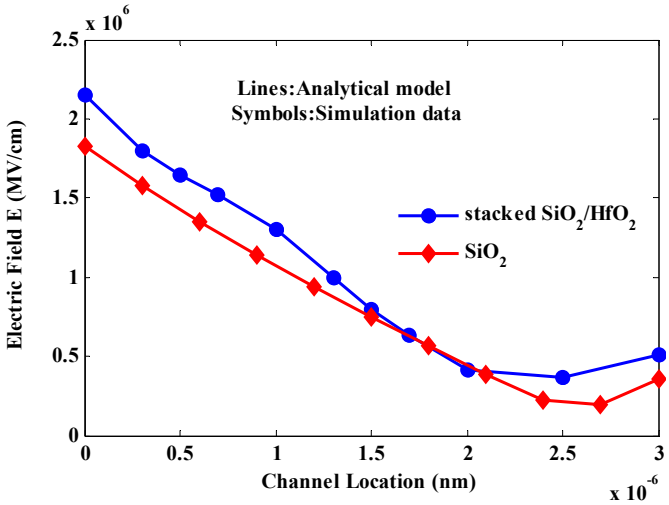

Fig. 6. Electric Field along the channel location for stacked high-k dielectric and SiO_2 with Vds=0.6V and Vgs=0.5V.

Table 2. Comparision table for electrical paramters in Stacked high-k dielectric and Silicon Dioxide.

Parameter		Stacked high-k dieelctic	Silicon dioxide
Surface Potential (V)	For L = 15 nm	1.925	0.715
Electric Field (MV/cm)	For L = 10 nm	1.432	1.151
Drain Current (A/μm)	For V_{gs} = 1 V	10^{-6}	10^{-8}

Table 2 shows the comparision table for the electrical parameters like Surface Potential, Electric Field and Drain current in SOI TFET with silicon dioxide and stacked oxide. Based on the data available in the Table 2 it shows a better results for the TFET device with stacked oxide.

CONCLUSION

In this paper, an analytical model for SOI TFET with a SiO_2/High-k stacked gate-oxide structure has been presented. The calculation is done by using 2-D Poisson's expression along with suitable boundary conditions using superposition

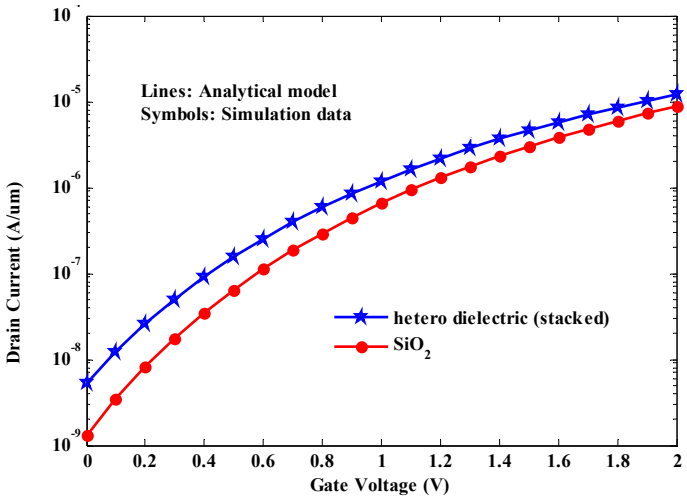

Fig. 7. Transfer characteristics in logarithmic scale for stacked high-k dielectric and SiO_2.

technique. The electrical characteristics such as surface potential, electric field (E) and drain current are modeled by considering all device parameters such as t_{ox}, t_{si}, L_{CH}, V_{gs} and V_{ds}. The analytical model is validated in TCAD 2D simulator and we obtained I_{DS} -V_{GS} characteristics by using BTBT rate generation (G). Compared to SiO_2, high k stacked gate oxide material improve the better performance of the compact device structure.

CONFLICT OF INTEREST

The authors declare that they have no competing interests.

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