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ORIGINAL ARTICLE

Representation of a nanoscale heterostructure dual material gate JL-FET with NDR characteristics

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Abstract

In this paper, we propose a new heterostructure dual material gate junctionless field-effect transistor (H-DMG-JLFET), with negative differential resistance (NDR) characteristic. The drain and channel material are silicon and source material is germanium. The gate electrode near the source is larger. A dual gate material technique is used to achieve upward band bending in order to access n-i-p-n structure which is caused by workfunction difference between electrodes and silicon. In JL-FETs as gate voltage increases, the electric-field intensifies and the band diagram profile starts to change. It is illustrated that, by increasing the gate voltage, the potential barrier decrease and the drain current increase. In the gate voltage of 0.64 V, due to appearance of a negative peak of electric-field and carriers transport within the field, the drain current decrease. Consequently, the NDR characteristic is achieved. With increase of the gate voltage the negative peak of electric-field is intensified and the drain current is decreased.

Keywords: *Dual Material Gate; Heterostructure; Junctionless Field Effect Transistor (H-DMG-JLFET); Negative Differential Resistance (NDR); Workfunction.*

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INTRODUCTION

Conventional field-effect transistors have junctions. These junctions can lead or prevent current flow by applying the gate bias voltage. The junctions are made of p and n type semiconductor. Other junctions could be made through connecting metal-semiconductor which is known as Schottky junction. BJTs and MOSFETs are made of p-n junctions; JFETs have only one kind of junction. The junctionless field-effect nanowire transistors (JL-FETs) have no junctions, which is a great advantage. Conventional FETs in nano diameters need high-doping concentration around 1×10^{19} cm^{-3} in two-types which faces challenges. In this event, the JL-FETs have one type doping in all regions. Since doping gradient between source and drain is zero, not only no diffusion occurs to limit fast annealing but also making short channel devices would be possible. To make a JL-FET, high-doping concentration is needed to allow current flow in ON state [1]. Choosing proper material in the gate is used to reduce gate resistance [2]. The threshold voltage of JL-FETs increases by doping concentration [3]. As this kind of transistors have no doping gradient, thermal budget in fabricating process would be reduced. These devices are like a heavily doped resistor that controls current flow through the gate voltage and are proper candidates for future nanometer devices [1-3].

First multi-gate nanowire transistors were introduced in 1996 [4]. These structures have better controllability on the channel through the gate and as a result, they have the most roll in SCEs [5]. Using dual material gate structures in JLFET to suppress OFF-state current is crucial [6]. These structures in FETs can reduce the thermal dependency of the threshold voltage due to little surface potential changing [7]. Dual material gate FETs have some advantages like higher Ion, Ion/Ioff than single material gate [8]. In recent years devices with negative differential resistance (NDR) characteristics have attracted noticeable

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attention [9-11]. Some of NDR functions are voltage-controlled oscillators [9, 10], Terahertz RTDs [11], logic circuits, high frequencies and memory devices [12]. For instance, intrinsic NDR characteristics in low voltage functions [9]. Further than RTDs, researchers tried a lot to achieve NDR in other devices. For example zigzag nanoribbon graphene has been introduced recently that has NDR characteristic which could be achieved by applying the controlled potential change on the gate of the device [12]. A tunneling field-effect transistor with vertical back layer graphene and Hexagonal-Bron-Nitride was brought forward that the resonant tunneling structure shows NDR characteristics [13].

Tri-terminal λ transistor with GaAs and a two channel GaAs by ð dopped on GaAs layer was also investigated[14]. Structures with Real-Space-Transfer (RST) [14-17] and NDR in graphene nanoribbon superlattice field-effect transistors were studied [18]. A new FET with NDR characteristics for low-power VLSI application was simulated [19]. A laboratory report for NDR and hysteresis phenomena in OLEDs based on graphene and its effects of device performance was done and concluded this two phenomena was because of graphene resistance [20].

Instabilities related to the hot carrier effects in a semiconductor have been investigated since 1940. NDR and ionization in the bulk semiconductor have led to devices such as Gunn diode and Optical Avalanche diode. Such instabilities related to hot carrier effects in low dimensional structures have attracted attention. By applying high enough electric field in a semiconductor, new kinds of instabilities could be seen that are not visible in bulk materials. Oscillatory related to high carrier effect is one of the study cases in hetero quantum- wells [21]. Obtaining these results with abovementioned theories are achievable by the new hetero quantum-well mechanism. The devices that use RST mechanism are used in high speed applications and high frequency performance [22]. One of the most common devices that can generate millimeter wavelengths is Gunn diode which NDR is achievable by it successfully. This device is used as a local oscillator and power amplifier in the ranges of 1 to 300 GHz, It is mentionable that devices with NDR could be used in micro-wave radars [23]. The important part of each electronic device is the material that appears some unique behaviors. For fabricating a high-frequency device, NDR should be produced in the material. One of the ways to reach this, are materials and system materials that contain two conduction bands , one band with higher electron mobility and the other one with lower electron mobility. Transferring carriers from the higher mobility band to the lower mobility band leads to NDR. By measuring I-V characteristic in a device which has proper ohmic contact, it could be understood that by applying an electric-field, its current would increase. In high electric-fields which devices with different materials are expected to be in ON state, by the continuous increment in electric field, current decreases in some devices, though NDR appears in I-V curve that changes the linearity of Ohms low [24]. Voltage-controlled NDRs are achieved in high electric fields [25]. In this paper, we represent a new JL-FET with NDR characteristic. The drain and channel material are silicon and source material is germanium. The gate electrode near the source is larger. Also, The NDR characteristic of proposed device has been investigated and analyzed.

EXPERIMENTALS

The cross section sketch of dual material JL-FET with NDR characteristic is shown in Fig. 1 It has 40 nm length and 14 nm width. The thickness of the silicon channel from silicon is 8 nm. Length of the germanium source is 5 nm and length of drain is 5 nm. By this definition we face a heterostructure JL-FET between source and channel. Germanium is one of the materials that have the potential to be used in the source side. Simulation studies show that Germanium has better ON state current in comparison with silicon [26]. It is also capable in fabricating process for transistors [27-30]. Germanium has some useful

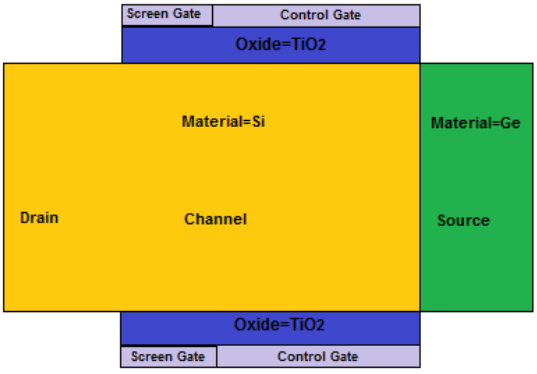

Fig. 1. Device structure.

advantages such as high mobility of electron (3900 cm^2/V s) and mobility of holes (1900 cm^2/V s) in room temperature, being strained in compound of silicon in semiconductor industry as a confirmed material in CMOS [31], and it has lack of conformity with silicon (%4) [32-35]. By the above mentioned characteristics, germanium has been used as a capable material in the source side. The gate dielectric layer is Tio_2 which it's effective oxide thickness (EOT) is 2 nm and has length of 30 nm. Using high-k dielectric is required for scaling of oxide thickness, high performance, improved ON state current, and Gate Induced Drain Leakage (GIDL) [36,37]. All regions are n-doped with concentration $1 \times 10^{19}\ cm^{-3}$ [38].

In our proposed structure the gate electrodes are made of two different metals with non-equal length. The electrode near the source which is called control gate (CG) with the length of 20 nm and the other electrode near drain which is called screen gate (SG) with the length of 10 nm. The workfunctions of CG and SG are equal to 4.7 eV and 4.0 eV, respectively. All simulations evaluated using 2D TCAD simulator Silvaco Atlas version 5.16.2.R [39]. We comprise the effect of Fermi-Dirac statistics in the calculation of the intrinsic carrier concentration required in the expressions of Shockley–Read–Hall (SRH) recombination. For thermal motion, CONMOB and Field-Effect mobility FLDMOB were used. Because of existence high doping concentration in the Source, Channel, and Drain; BGN and Auger were chosen [40].

RESULTS AND DISCUSSIONS

Fig. 2 shows the drain current of the proposed device. By increasing the gate voltage, the drain current increases, but in the gate voltage of 0.64 V, the I-V characteristic treatment is changed. Base on This change of behavior the voltage-controlled NDR is illustrated. For investigating the reason of NDR the energy band diagram and the electric field profile are calculated.

The OFF-state of device is assumed for zero gate voltage. Fig. 3 shows the OFF state energy band diagram of the proposed device. This implicates the device is n-i-p-n junction like due to energy band gap of germanium and silicon, and different workfunction of electrodes which have different length [41]. In zero bias of the gate, the device is fully depleted and there is no conduction mechanism [42].

The ON-state energy band diagrams at gate voltages of 0.63, 0.64 and 0.65 V are shown in Fig. 4. This figure indicates that the band diagram profile starts to change for gate voltage more than 0.64 V.

Fig. 5 illustrates the electric-Field changes of proposed device in the gate voltage of 0.63, 0.64 and 0.65 V. As know the negative peak of electric-field reduces electron velocity [43]. In high electric fields mobility of carriers would be field dependent. As electric field increases, drift velocity decreases [44, 45]. It is shown that in the gate voltage of

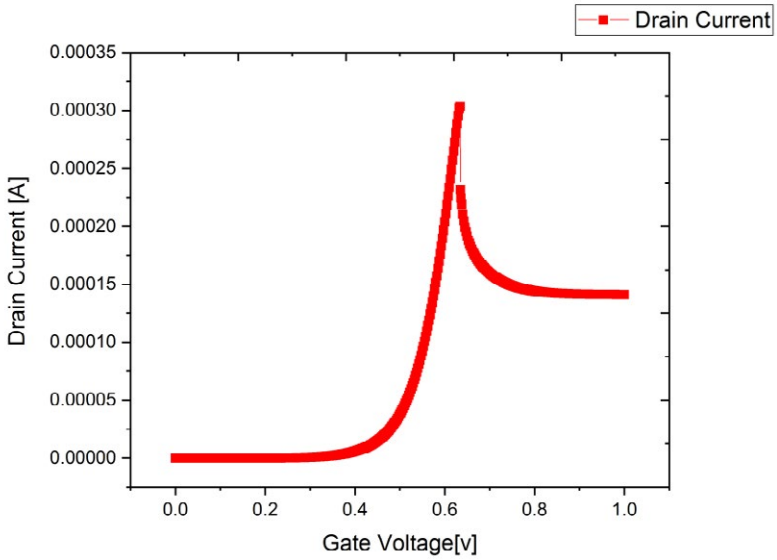

Fig. 2. Drain current- Gate voltage with NDR characteristic.

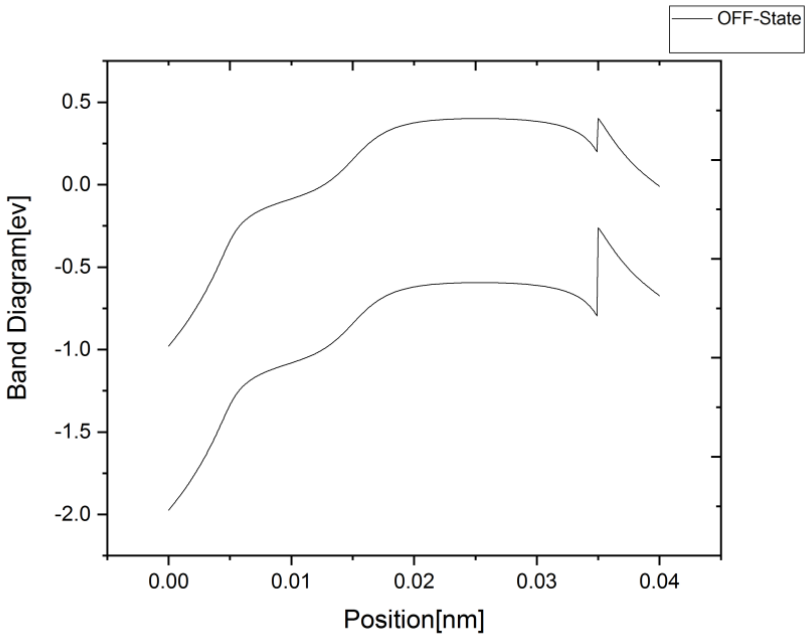

Fig. 3. The OFF-state energy band diagram of the proposed device as shown in Fig. 1.

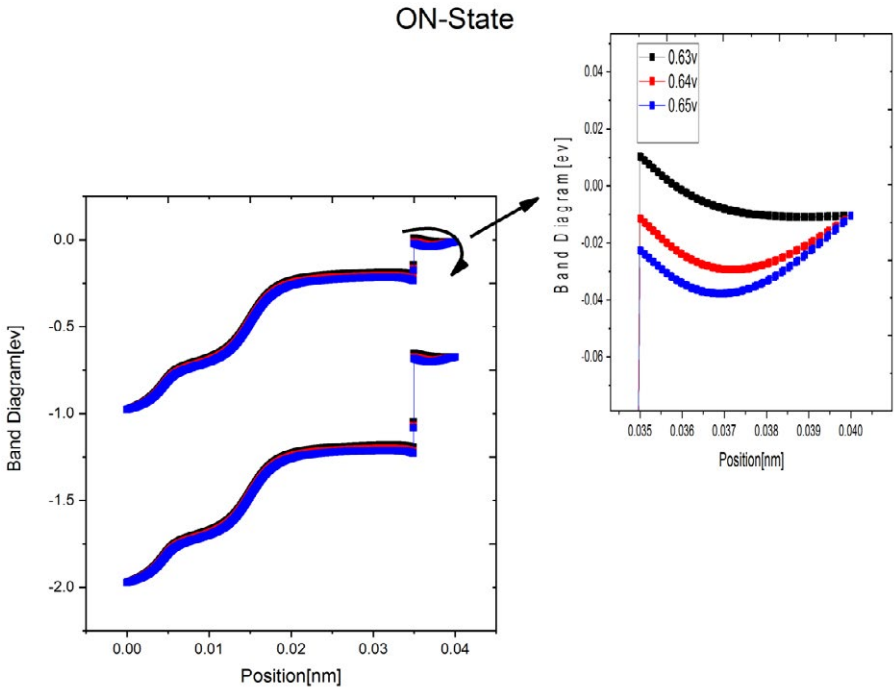

Fig. 4. The ON-state energy band diagram for the gate voltages 0.63 V, 0.64 V, and 0.65 V.

0.64 V, due to appearance of a negative peak of electric-field and carriers transport within the field, the drain current decrease. Consequently, the NDR characteristic is achieved. For increasing of the gate voltage the negative peak of electric-field is amplified and consequently, the electron mobility and velocity and so the drain current are decreased [46].

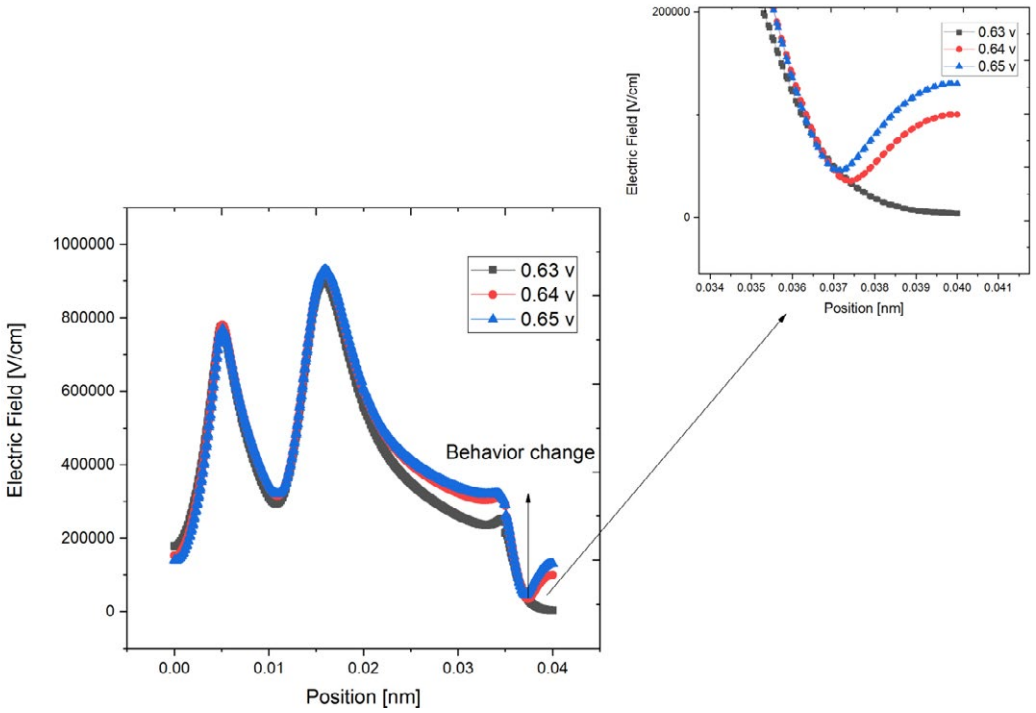

Fig. 5. The electric field profile in the gate source of 0.63 V, 0.64 V, and 0.65 V.

CONCLUSION

In summary, we proposed a new hetero-structure dual material gate junctionless field-effect transistor (H-DMG-JLFET), with negative differential resistance (NDR) characteristic. In this device the gate electrode near the source is larger than the gate electrode near the drain. Due to appearance of a negative peak of electric-field and carriers transport within the field, the drain current decrease by the gate voltage increase. Consequently, the NDR characteristic is exhibited . The proposed device would be a promising structure for achieving NDR in JL-FETs.

DISCLOSURE STATEMENT

All authors declare that they have no conflict of interest in the publication of this manuscript.

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