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ORIGINAL ARTICLE

Performance evaluation of Carbon nanotube junctionless tunneling field effect transistor (CNT-JLTFET) under torsional strain: A quantum simulation study

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Abstract

In this paper, the performance of a CNT-JLTFET under different values of torsional strains of 0, 3, and 5 degrees has been investigated. Simulation has been carried out using non-equilibrium Green's function (NEGF) formalism in the mode-space approach and in the ballistic limit. The simulation results indicate that, under torsional strain, an increase occurs in the energy band-gap, and thus the on- and off-currents are reduced, thought that reduction has a greater percentage in the off-current, resulting in the increase in the ON/OFF current ratio. Besides, the switching characteristics of the device including power-delay product (PDP) and intrinsic delay (τ) have been studied.

Keywords: *Band-Structure-Limited Velocity; Intrinsic Delay (τ); Mode-Space; Power-Delay-Product (PDP); Torsional Strain.*

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INTRODUCTION

By reducing the channel length to lower than 20 nm, fabrication of the conventional MOSFETs is facing serious problems due to the need for ultra-steep doping profile at the drain and source junction regions [1, 2].

Stringent demands on fabrication has rendered any further scaling of the MOSFETs almost impossible [3, 4]. Therefore, for devices with a channel length below 20 nm, junctionless transistors (JLT) are needed. Junctionless transistors are a reliable device for the future technology since they reduce complexities and as much the fabrication costs [5]. In order to optimize the JLT performance, some new design methods such as SOI-JLT, gate all around, bulk planer JLT and nano wire JLT have been proposed [6-10].

The MOSFETs capability for switching from the off to the on-state has been shown by the slope of the I_D-V_{GS} characteristic curve in sub-threshold performance region, which is called sub-threshold slope. The sub-threshold slope (ss) in the MOSFETs is limited thermally to $60\frac{mV}{dec}$ while it is possible to reach a sub-threshold slope below $60\frac{mV}{dec}$ using alternative transistors such as tunneling field-effect transistors (TFET) [11, 12]. Although conventional TFETs have a better sub-threshold slope than the MOSFET structures, but they also have a lower on-current [13, 14].

Carbon nanotubes (CNTs) and graphene nanoribbons (GNRs) have unique properties, such as very low effective mass, direct energy band-gap, low thickness and high mobility of electrons and holes, making them suitable for band-to-band tunneling (BTBT) devices applications [15-19].

Strain engineering is a method for changing the energy band-gap in carbon nanotubes and graphene nanoribbons [20]. Effects of the uniaxial strain and torsional strain on the performances of the conventional MOSFETs, TFETs and MOS-like JLTs have been investigated [21, 22]. According to the results, the uniaxial and torsional strains can affect the electrical properties of the devices since

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they change the energy band-gap, band-structure-limited velocity and density of states (DOS) of carriers in CNTs and GNRs.

The present study has explored the torsional strain effects on the performance of a CNT-based tunneling field-effect transistor. The effects of torsional strain on the on-current, off-current, intrinsic delay (τ), and power-delay product (PDP), have also been discussed and analyzed.

This paper is organized as follows. The device structure and simulation method are introduced in Section 2. The simulation results are presented and discussed in Section 3. Finally, this paper is concluded with a conclusion in Section 4.

DEVICE STRUCTURE AND SIMULATION METHOD

Fig. 1 shows the structure of the carbon nanotube junctionless tunneling field-effect transistor (CNT-JLTFET). Each of the source, channel and drain regions has the same length of 15 nm. A zigzag single-walled carbon nanotube with chirality (16, 0) is used throughout the structure. Due to the junctionless structure of the transistor, a uniform N-type doping profile with a high concentration of $10^9\, m^{-1}$ is used for the source, channel, and drain. The structure involves two separate gates isolated from each other by a SiO_2 layer, called a spacer, with a dielectric constant of $\varepsilon_{OX} = 3.9$ and a length of 3 nm. In the other regions, HfO_2 with a dielectric constant of $\varepsilon_{OX} = 16$ is used as an oxide. The work function of gate materials is chosen to be similar to that of the carbon nanotube. The main gate is the control gate (CG), which modulates the width of the tunneling potential barrier. The polarity gate (PG) with a constant voltage of -0.8 V and a length of 12 nm is used to create a P^+ region as the source region. The charge plasma or electrically activation concept (method) is a conventional method wherein the desired doping profile is created by applying an appropriate external bias voltage for polarity gate (P-Gate).

In order to simulate the above coaxial structure, the non-equilibrium Green's function (NEGF) procedure in the ballistic regime and with an uncoupled mode-space approach has been employed**.** In this method, the Poisson and Schrödinger equations are solved in a self-consistent manner [23, 24]. In order to calculate the potential distribution of the device, the Poisson equation in cylindrical coordinates [25] through the finite difference discretization approach is changed to a set of nonlinear equations, which are subsequently solved by the Newton-Raphson method [26].

Now, the Green's function for *q*-th mode is calculated by the potential distribution as follows [24]:

$$G_q = \left[(E + i0^+)I - H_q - \Sigma_{Sq} - \Sigma_{Dq} \right]^{-1} \quad (1)$$

where, *E*, *0⁺*, *I* and *Hq* are energy, a positive infinitesimal number, the identity matrix and the Hamiltonian matrix of the isolated channel for the *q*-th mode, respectively. The connection between the source and the drain with the channel is modeled by two self-energy matrices Σ_{Sq} and Σ_{Dq}, respectively.

The tight-binding approximation with only one P_z orbital for each atom is used to get the Hamiltonian matrix for *q*-th mode, as follows [27]:

$$H_q = \begin{bmatrix} U_1 & b_{2q} & 0 & 0\ldots0 \\ b_{2q} & U_2 & b_{1q} & 0\ldots0 \\ \ddots & & \ddots & \ddots \end{bmatrix} \quad (2)$$

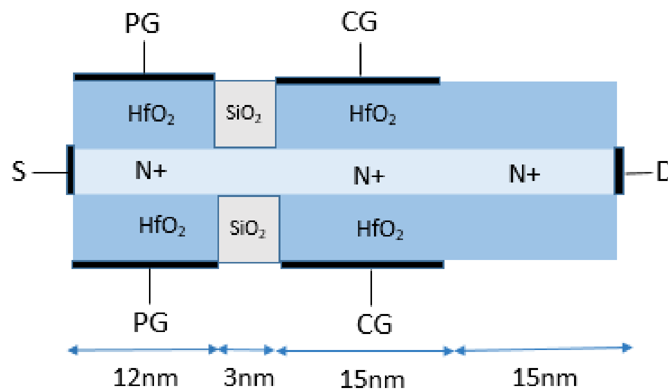

Fig. 1. Schematic view of a CNT-JLTFET.

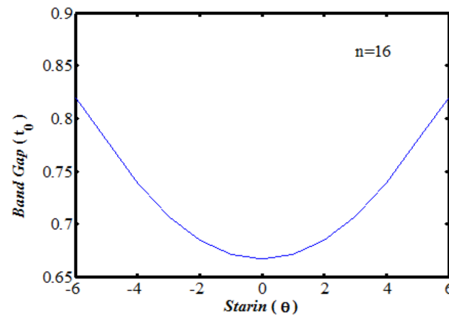

Fig. 2. Band-gap versus torsional strain for CNTs with chirality (16, 0).

where U_i is the potential in the i-th ring and t_0, $b_{1q}=t_0$ and $b_{2q}=2t\cos\left(\frac{\pi q}{n}\right)$ are the coupling values between two adjacent carbon atoms and two farther and two nearer adjacent rings, respectively.

The self-energy matrices are obtained in the ohmic contact approximation, which models the contacts as semi-infinite metallic nanotubes [25].

In order to introduce the torsional strain into the NEGF procedure, the suggested method in Ref. [28] is utilized. By applying torsional strain, the change in the carbon nanotube bond vectors [20] leads to the change of the hopping parameters by the Harrison's formula [29], and therefore the mode-space coupling parameters in the Hamiltonian matrix are altered as follows:

$$b_{1q} = t_0 \cos^2(\theta) \tag{3}$$
$$b_{2q} = t_0 \left| \frac{4}{1+(\sqrt{3}+\tan\theta)^2} + \frac{4}{1+(\sqrt{3}-\tan\theta)^2}\, e^{-i\frac{2\pi q}{n}} \right|$$

b_{1q} and b_{2q} are the coupling vectors of two farther and nearer adjacent rings, respectively. Besides, t_0 signifies the C-C hopping parameter, which is equal to 2.7 eV in the unstrained state.

In this study, the torsional strain angle θ is considered to be lower than 5° due to the linear response of the carbon nanotube in this range of torsion angles [28].

Based on relation $\nu = -\frac{\left(\frac{\Delta r}{r}\right)}{\left(\frac{\Delta l}{l}\right)} = -\frac{\varepsilon_c}{\varepsilon_t}$, the Poisson's ratio is defined as the ratio of the circumferential strain (ε_c) to the transverse strain (ε_t) [30]. r and l are the radius and length of the carbon nanotube in the unstrained state, respectively, and Δr and Δl are the radius and length changes of the carbon nanotube after applying strain. Since torsional strain also causes a transverse strain, the carbon nanotube radius is also modified by the torsional strain according to the Poisson's ratio. In this study, ν is assumed to be 0.2 [28].

After calculating the Green's function by Eq. (1), the local density of states due to the source and drain contacts are calculated according to Eq. (4) as follows:

$$D_{Sq(Dq)} = G_q \Gamma_{Sq(Dq)} G_q^{\dagger} \tag{4}$$

where $\Gamma_{Sq(Dq)} = i(\Sigma_{Sq(Dq)} - \Sigma^{\dagger}_{Sq(Dq)})$ is the source (drain) broadening function. Finally, the charge density filled by each contact is calculated by the following equation:

$$Q_{Sq(Dq)}(z) = -e\int_{E_N}^{\infty} D_{Sq(Dq)}(E,z) f(E-E_{FS(D)})dE + e\int_{-\infty}^{E_N} D_{Sq(Dq)}(E,z)(1-f(E-E_{FS(D)}))dE \tag{5}$$

where e and E_N are the electron charge and the energy neutralization level, respectively. The charge density in the channel resulting from q-th mode is calculated by the sum of the $Q_{Sq}(z)$ and $Q_{Dq}(z)$. The sum of the charges resulting from all modes is used as input to the Poisson equation to predict a better estimate of the potential distribution. This loop between the Poisson's equation and NEGF formalism is solved, self-consistently. After approaching convergence and reducing the error to the desired value, the current is calculated as follows:

$$I_q(E) = 2\times\frac{2_e}{h}\times\int_{-\infty}^{+\infty} T_q(E)\left[f_s(E)-f_D(E)\right]dE \tag{6a}$$

$$I = \sum_q I_q \tag{6b}$$

where $T_q(E) = Trace(\Gamma_{Sq} G_q \Gamma_{Dq} G_q^{\dagger})$ represents the transfer probability of a carrier with the energy E between two contacts of the source and drain resulting from q-th mode.

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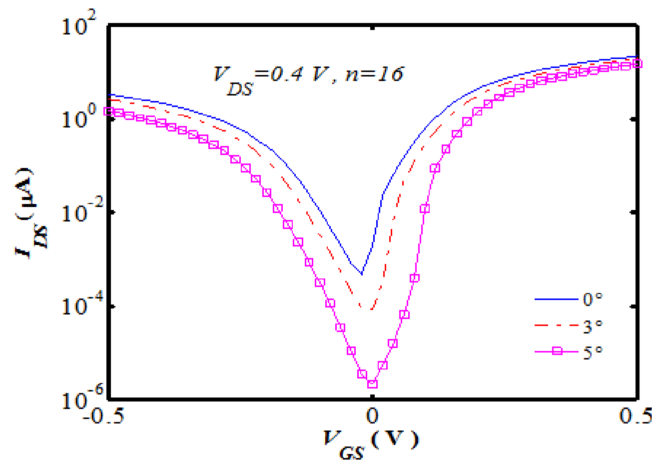

Fig. 3. I_D-V_{GS} characteristics of the CNT-JLTFET for different values of torsional strain at V_{DS}=0.4 V.

This procedure has been implemented in MATLAB, and the accuracy of the program was also confirmed in our previous works [22, 31].

RESULTS AND DISCUSSION

Fig. 2 represents the diagram of energy band-gap in terms of torsional strain for a carbon nanotube with a chirality of (16, 0). As this figure shows, by increasing the degree of torsional strain, the energy band-gap in the carbon nanotube increases.

Fig. 3, illustrates the I_D-V_{GS} characteristic of the junctionless tunneling transistor introduced in the previous section for different values of torsional strain (0°,3°,5°) at V_{DS}=0.4 V. As shown by this figure, by increasing the torsional strain, the off and am-bipolar current decreases. To explain this behavior, diagrams of the carrier density at different energy levels along the device at the off-state (V_{DS}=0.4 V and V_{GS}= -0.4 V) have been depicted under the strain-free and torsional strains of 3° and 5° in Figs. 4(a), (b), and (c), respectively. The off-current and am-bipolar behavior of the tunneling FET are caused by the tunneling of the carries from the valence band of the channel to the conduction band of the drain. As is clear from Fig. 2, by increasing the torsional strain, the energy band-gap increases, which in turn increases the width of the tunneling barrier on the drain-channel side resulting and in a reduction tunneling leakage and am-bipolar current.

In the following, in Fig. 5, the I_D-V_{DS} characteristic of the junctionless transistor at V_{GS}=0.4 V has been simulated. As it is clear from this figure, the on-current has been decreased by increasing the torsional strain. Similarly, this behavior can also be explained by depicting carriers density at different energies along the device in the on-state for the typical voltage of V_{DS}=0.4 V and V_{GS}=0.4 V. Figs. 6 (a), (b), and (c) represent the strain-free and torsional strains of 3^0 and 5^0, respectively.

The on-current in the tunnel structure is caused by the tunneling of the carriers from the valence band of the source to the conduction band of the channel and their moving towards the drain. As the torsional strain is increased, the tunneling barrier width on the source-channel extension increases and hence the on-current is reduced.

For further comparison, the $\frac{I_{ON}}{I_{OFF}}$ diagram in terms of the on-current at a specific bias point, V_{DS}=0.4 V, has been given in Fig. 7. As is evident, by increasing the torsional strain, the ON/OFF current ratio increases and the above-mentioned tunnel structure for a strain of 5° has a considerably higher ON/OFF current ratio compared to the other states.

Finally, in order to demonstrate the effect of applying torsional strain on the switching properties of the aforementioned device, the intrinsic delay (τ) and *PDP* in terms of $\frac{I_{ON}}{I_{OFF}}$ for different values of torsional strain are respectively given in Figs. 8 (a) and (b). In order to simulate the effect of torsional strain on the switching characteristics of the device, the approach used in Ref. [32] has been adopted. The intrinsic delay has been calculated based on the relation $\tau = C_G V_{DD} = \frac{\Delta Q}{I_{ON}}$, which ΔQ is the charge variation throughout the device in any switching event. According to Fig. 8 (a), the intrinsic delay at a given $\frac{I_{ON}}{I_{OFF}}$ ratio is an increasing function of the torsional strain. This issue can be justified by

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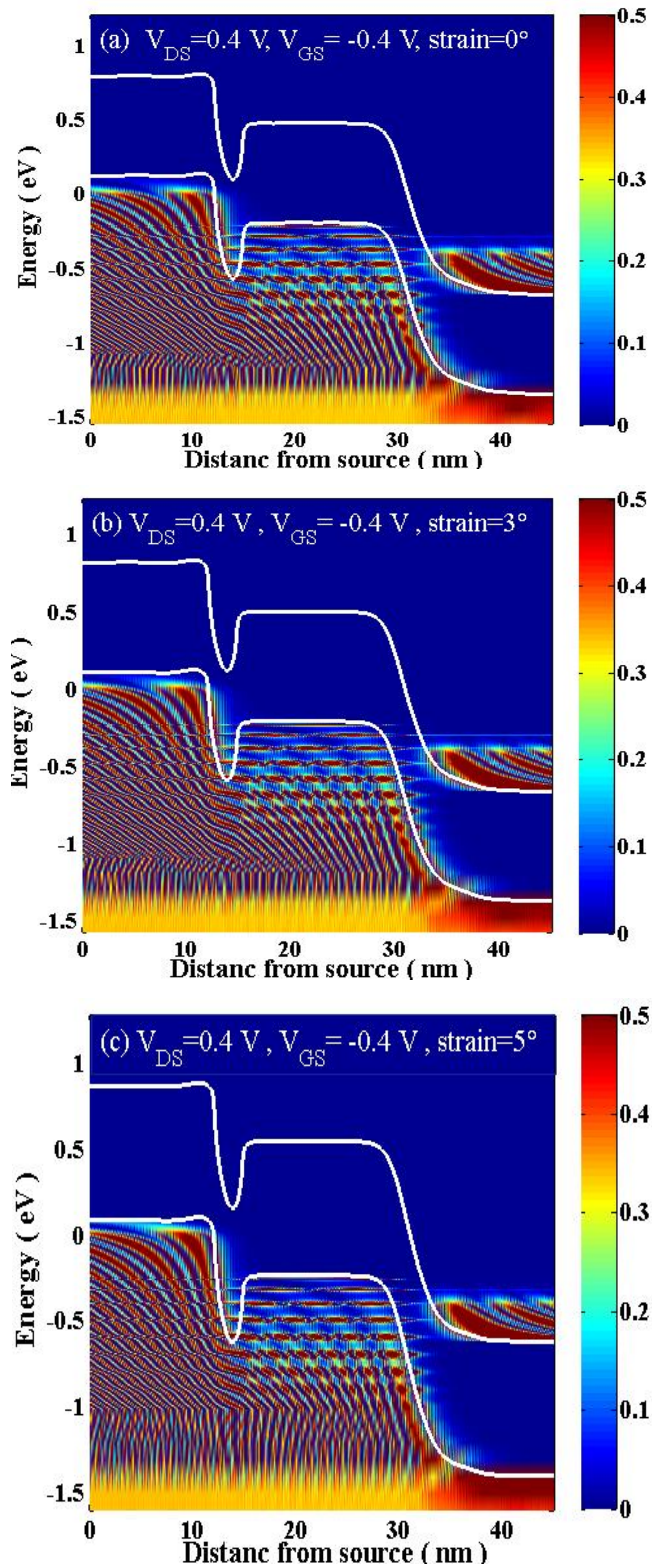

Fig. 4. Energy band diagram (white lines) and the carriers density along the CNT-JLTFET in the off-state for different values of torsional strain (a) $\theta = 0^0$, (b) $\theta = 3^0$ and (c) $\theta = 5^0$. The scale bars on the right indicate the density of electrons.

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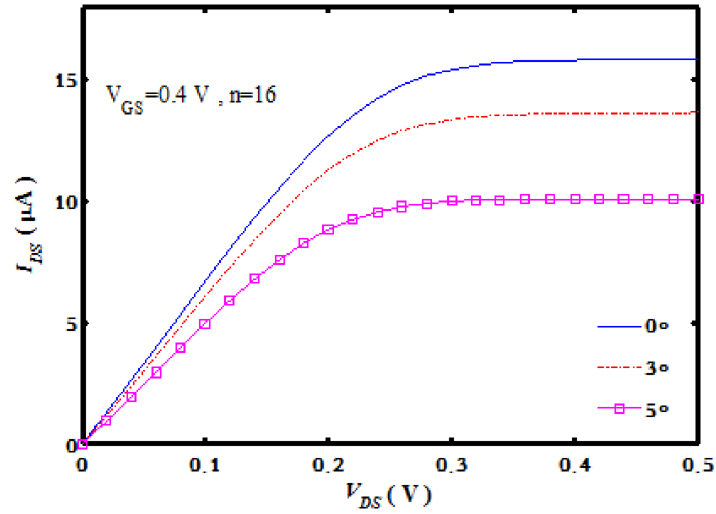

Fig. 5. I_D-V_{DS} characteristics of the CNT-JLTFET for different values of torsional strain at V_{GS}=0.4 V.

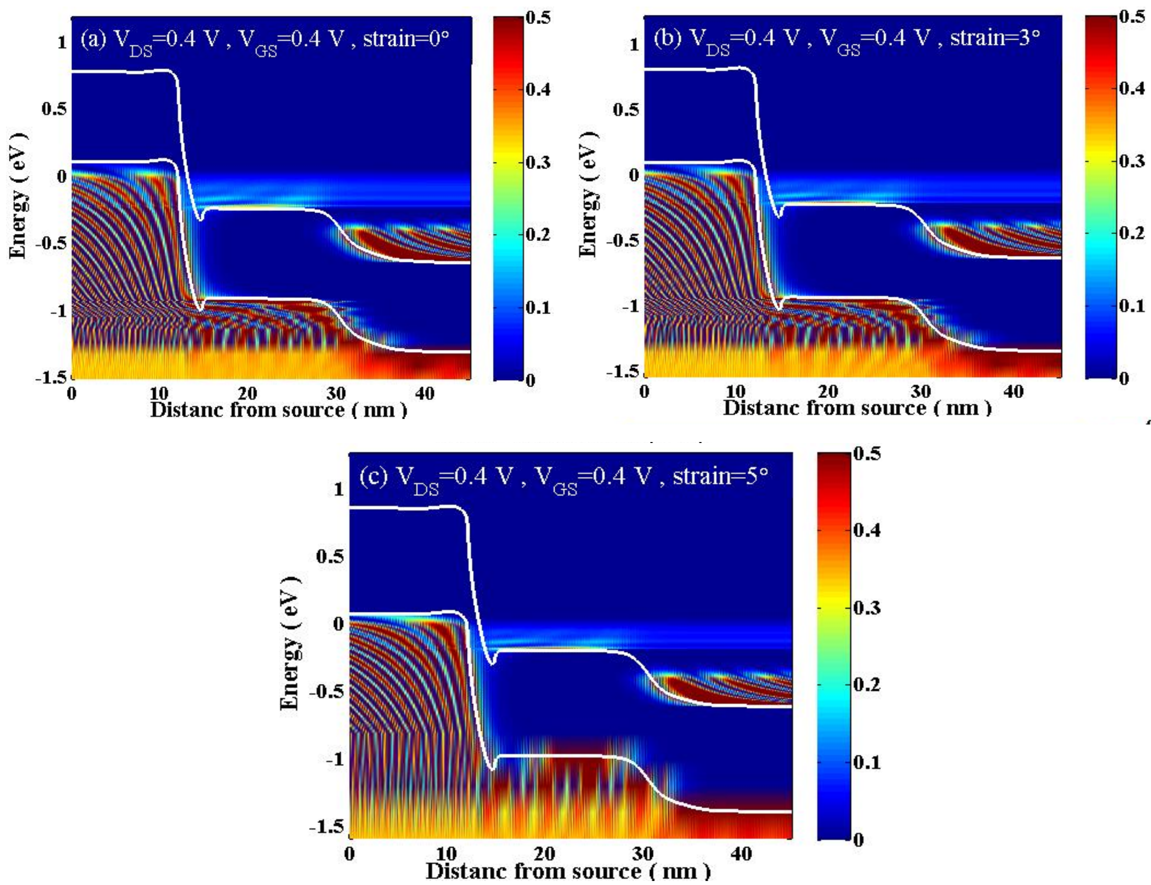

Fig. 6. Energy band diagram (white lines) and the carriers density along the CNT-JLTFET in the on-state for different values of torsional strain (a) $\theta = 0^0$, (b) $\theta = 3^0$ and (c) $\theta = 5^0$. The scale bars on the right indicate the density of electrons.

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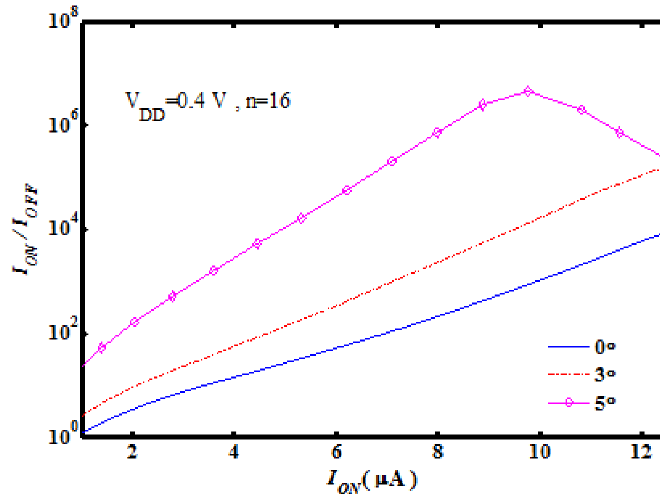

Fig. 7. $\frac{I_{ON}}{I_{OFF}}$ ratio versus I_{ON} for a CNT-JLTFET under different values of torsional strain at V_{DS}=0.4 V.

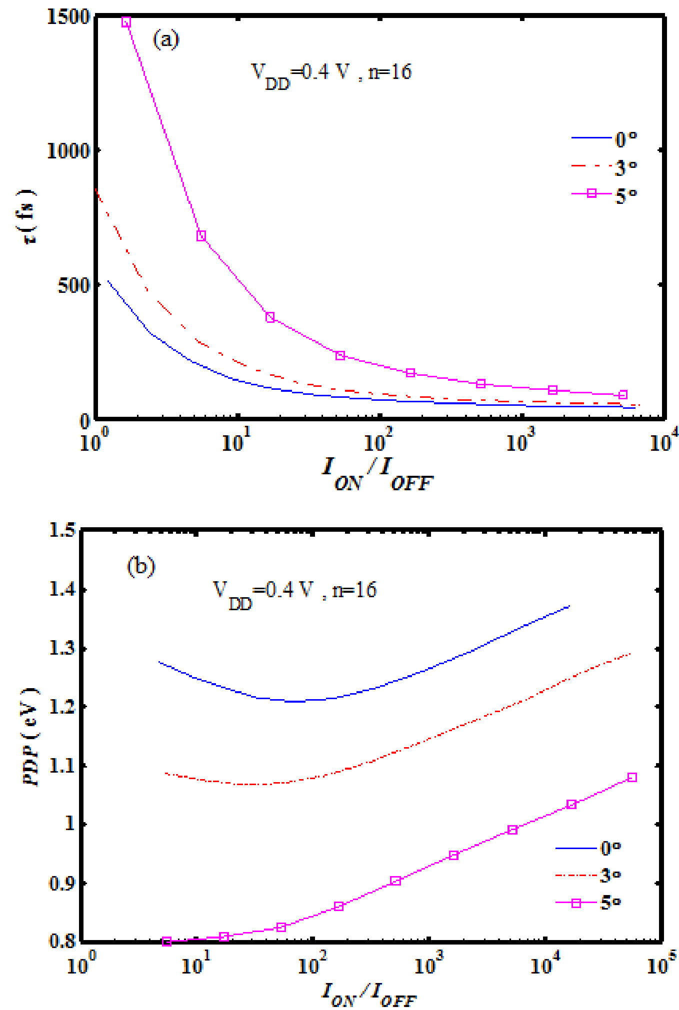

Fig. 8. Illustration of (a) intrinsic delay and (b) PDP versus $\frac{Ion}{Ioff}$ for a CNT-JLTFET under different values of torsional strain.

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referring to Fig. 7. As this figure shows, in a given $\frac{I_{ON}}{I_{OFF}}$ ratio, by increasing the value of the torsional strain imposed on the device, the on-current and therefore the charge and discharge speed of the gate capacitance are reduced. Therefore, the intrinsic delay increases. Another reason for this behavior is the reduction of the band-structure-limited velocity, due to the torsional strain, in the chirality of the carbon nanotube (*n*=3p+1) used in this structure, which reduces the velocity of the carriers in the device and resultantly increases the intrinsic delay.

PDP is defined based on the relation $PDP = \Delta Q \, .V_{DD} = \tau . I_{ON} \, .V_{DD}$. As shown in Fig. 8 (b), *PDP* is a decreasing function of the torsional strain. This can be justified by the reduction of ΔQ due to the torsional strain. Moreover, the dominant effect of the on-current reduction with respect to the increase of the intrinsic delay is another reason for this behavior.

CONCLUSION

Numerical studies on carbon nanotube junctionless TFET (CNT-JLTFET) have indicated that due to the torsional strain, band gap and band structure limited velocity have changed. Accordingly, under torsional strain, as compared to an unstrained case, both on- and off-currents have decreased but the ON/OFF current ratio has increased. Power-delay product (PDP) and intrinsic delay (τ) have also been investigated. Simulation results show that under torsional strain, τ and PDP have increased and decreased, respectively.

CONFLICT OF INTEREST

The authors declare that they have no competing interests.

REFERENCES

[1] Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., Colinge J.-P., (2009), Junctionless multigate field-effect transistor. *Appl. Phys. Lett*. 94: 053511.

[2] Kumar M. J., Janardhanan S., (2013), Doping-less tunnel field effect transistor: Design and investigation. *IEEE Trans. Electron Devices*. 60: 3285-3290.

[3] Coquand R., Barraud S., Cassé M., Leroux P., Vizioz C., Comboroure C., Perreau P., Ernst E., Samson M.-P., Maffini-Alvaro V., (2013), Scaling of high-κ/metal-gate TriGate SOI nanowire transistors down to 10 nm width. *Solid State Electron*. 88: 32-36.

[4] Park J.-T., Colinge J.-P., (2002), Multiple-gate SOI MOSFETs: device design guidelines. *IEEE Trans. Electron Devices*. 49: 2222-2229.

[5] Colinge J.-P., Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., Razavi P., O'neill B., Blake A., White M. J. N. N., (2010), Nanowire transistors without junctions. *Nat. Nanotechnol*. 5: 225-229.

[6] Han M.-H., Chang C.-Y., Chen H.-B., Wu J.-J., Cheng Y.-C., Wu, Y.-C., (2013), Performance comparison between bulk and SOI junctionless transistors. *IEEE Electron Device. Lett.* 34: 169-171.

[7] Gundapaneni S., Ganguly S., Kottantharayil A., (2011), Bulk planar junctionless transistor (BPJLT): An attractive device alternative for scaling. *IEEE Electron Device. Lett.* 32: 261-263.

[8] Su C.-J., Tsai T.-I., Liou Y.-L., Lin Z.-M., Lin H.-C., Chao T.-S, (2011), Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels. *IEEE Electron Device. Lett.* 32: 521-523.

[9] Ávila-Herrera F., Paz B., Cerdeira A., Estrada M., Pavanello M., (2016), Charge-based compact analytical model for triple-gate junctionless nanowire transistors. *Solid State Electron.* 122: 23-31.

[10] Bozorgi Golafzani, A., Sedigh Ziabari S. A., (2020), Representation of a nanoscale heterostructure dual material gate JL-FET with NDR characteristics. *Int. J. Nano Dimens*. 11: 12-17.

[11] Zhang Q., Zhao W., Seabaugh A., (2006), Low-subthreshold-swing tunnel transistors. *IEEE Electron Device. Lett*. 27: 297-300.

[12] Ahangari Z., (2019), Novel attributes of steep-slope staggered type heterojunction p-channel electron-hole bilayer tunnel field effect transistor. *Int. J. Nano Dimens*. 10: 391-399.

[13] Koswatta S. O., Lundstrom M. S., Nikonov D. E., (2009), Performance comparison between pin tunneling transistors and conventional MOSFETs. *IEEE Trans. Electron Devices.* 56: 456-465.

[14] Palanichamy V., Kulkarni N., Thankamony Sarasam A. S., (2019), Improved drain current characteristics of tunnel field effect transistor with heterodielectric stacked structure. *Int. J. Nano Dimens*. 10: 368-374.

[15] Novoselov K., Morozov S., Mohinddin T., Ponomarenko L., Elias D., Yang R., Barbolina I., Blake P., Booth T., Jiang D., (2007), Electronic properties of graphene. *Phys. Status Solidi (b)*. 244: 4106-4111.

[16] Ghoreishi S. S., Yousefi R., (2017), A computational study of a novel graphene nanoribbon field effect transistor. *Int. J. Mod. Phys. B.* 31: 1750056 (14 pages).

[17] Tamersit K., (2019), A new ultra-scaled graphene nanoribbon junctionless tunneling field-effect transistor: Proposal, quantum simulation, and analysis. *J. Comput. Electron*. 1-7.

[18] Tahaei S. H., Ghoreishi S. S., Yousefi R., Aderang H., (2019), A computational Sstudy of a heterostructure tunneling Carbon nanotube field-effect transistor. *J. Electron. Mater*. 48: 7048-7054.

[19] Tamersit K., (2020), Computational study of pn Carbon nanotube tunnel field-effect transistor. *IEEE Trans. Electron Devices*. 67: 704-710.

[20] Yang L., Anantram M., Han J., Lu, J., (1999), Band-gap change of carbon nanotubes: Effect of small uniaxial and torsional strain. *Phys. Rev. B*. 60: 13874-13878.

[21] Sheikhi M. H., (2009), Effect of strain on the performance of MOSFET-like and p–i–n carbon nanotube FETs. *Solid State Electron*. 53: 497-503.

[22] Pourian P., Yousefi R., Ghoreishi S. S., (2016), Effect of uniaxial strain on electrical properties of CNT-based

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junctionless field-effect transistor: Numerical study. *Superlat. Microstruct.* 93: 92-100.

[23] Venugopal R., Ren Z., Datta S., Lundstrom M. S., Jovanovic D., (2002), Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches. *J. Appl. Phys.* 92: 3730-3739.

[24] Guo J., Datta S., Lundstrom M., Anantam M., (2004), Toward multiscale modeling of carbon nanotube transistors. *Int. J. Multiscale Com.* 2: 257–276.

[25] Guo J., (2004), Carbon nanotube electronics: modeling, physics, and applications. *Purdue University*.

[26] Ren Z., (2001), Nanoscale MOSFETs: Physics, simulation, and design. *Purdue University*, 41-64.

[27] Datta S., (1997), *Electronic transport in mesoscopic systems*. Cambridge university press.

[28] Yoon Y., Guo J., (2007), Analysis of strain effects in ballistic carbon nanotube FETs. *IEEE Trans. Electron Devices.* 54: 1280-1287.

[29] Harrison W., (1989), Electronic structure and the properties of solids. The physics of the chemical bond., ch. 11, Mixed tetrahedral solids. Dover Publications, Inc.

[30] Natsuki T., Tantrakarn K., Endo M., (2004), Effects of carbon nanotube structures on mechanical properties. *Appl. Phys. A*. 79: 117-124.

[31] Yousefi R., Ghoreishi S. S., (2012), A computational study of strain effects in the band-to-band-tunneling carbon nanotube field-effect transistors. *Int. J. Mod. Phys. B.* 26: 1250155.

[32] Faraji M., Ghoreishi S. S., Yousefi R., (2018), Gate structural engineering of MOS-like junctionless Carbon nanotube field effect transistor (MOS-like J-CNTFET). *Int. J. Nano Dimens.* 9: 32-40.

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