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ORIGINAL ARTICLE

Conventional vs. junctionless gate-stack DG-MOSFET based CMOS inverter

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Abstract

In this article, the high-k gate dielectric effect on the operation of complementary metal oxide semiconductor (CMOS) inverter build using conventional (CL) double-gate (DG) metal oxide semiconductor field effect transistor (MOSFET) and junctionless (JL) double-gate (DG) MOSFET has been explored. It is found that the improvement in inverter performance is more pronounced in CL-DG-MOSFET based CMOS inverter in comparison to JL-DG-MOSFET based CMOS inverter when SiO_2 is replaced by the high-k dielectric at gate oxide. The improvement in low noise margin (ΔNML), high noise margin (ΔNMH), gain (ΔA) & propagation delay (ΔP_d) is 3.19%, 1.64%, 5.2% & 0.9% respectively when SiO_2 is replaced by TiO2 at gate oxide in case of CL-DG-MOSFET based CMOS inverter whereas it is 1.96%, 1.24%, 3.4% & 1.71% respectively in case of JL-DG-MOSFET based CMOS inverter. Consequently, the utilization of high-k dielectric as gate oxide is more advantageous in CL-DG-MOSFET devices for improved stability and gain of CMOS inverter.

Keywords: *CMOS Inverter; DG-MOSFET; Gate-Stack; High-k; Junctionless.*

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INTRODUCTION

The performance improvement of integrated circuits made a successful demand in semiconductor industries. This is achieved owing to the unremitting scaling of the semiconductor device which has been reached into the nanometer regime. However, due to aggressive scaling of the device's dimensions numerous short channel effects (SCEs) are in the limelight. The multi-gate architecture is an effective approach to condense these SCEs owing to more channel's controllability. In accordance with the device performance, various hybrid topologies like double gate (DG), triple gate, gate all around (multi-gate) metal oxide semiconductor field effect transistors (MOSFETs) were invented to reduce the SCEs [1-4].

In the nanoscale era, the creation of an ultra-sharp junction is an additional restraint in the deep downscaling of the FET devices. To iron out this problem, Colinge *et al.* [5] projected the concept of junctionless (JL) transistors. Further, to follow the prediction provided by the international technology roadmap for semiconductor (ITRS), [6] recent research elaborates several device engineering schemes to enhance the performance of scaled devices by minimizing SCEs & maintaining the electrical characteristics constant. By this, the integration level of Nano-

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electronic devices is enhancing linearly. The gate oxide layer, that is, silicon dioxide (SiO_2) has also been decreased to a few nanometer thicknesses thereby maintaining the device performance constant. However, if the thickness is scaled lower than 1 nm, quantum tunneling effects will start to dominate and the problems arise in power consumption [7-9]. Technically these issues are overcome by owning high dielectric materials (high-*k*) as gate oxide. The key reason to prefer high-*k* materials for Nano-devices is that the thickness of the high-*k* dielectric materials increases with the same capacitance. They induce a larger bandgap and larger dielectric constant. The use of high-k materials decreases the gate leakage current flowing through the device at a higher rate along with reducing static power consumption. Thus, high-k dielectrics will be most likely implemented in advanced semiconductor devices in combination with metal gates instead of the poly-Si gates. With this prominence, high-*k* materials are well suitable to improvise the device characteristics [10-12]. Further, Titanium dioxide (TiO_2) is said to be one of the most promising high-*k* dielectrics for the next-generation CMOS device applications due to its relatively high dielectric constant and superior thermodynamic stability [13-14].

Further, when high-*k* dielectrics are positioned precisely on silicon, they could regress the FETs performance owing to feeble interface condition. To toss out this issue, gate-stack (GS) technology is conveyed by researchers [15-16]. In this technology, a thin SiO_2 layer is inserted between the silicon substrate and the high-*k* gate dielectric layer. This helps in preserving the quality of the Si/SiO_2 interface as well as in reducing the gate tunneling current simultaneously.

In this article, a 2D Sentaurus TCAD mixed-mode simulator is utilized to investigate the high-*k* gate dielectric effect on the CMOS inverter performance build using conventional (CL) & junctionless (JL) DG-MOSFET devices. The organization of this manuscript is ordered as follows: The paper starts with an introduction as section 1 and the device description with the simulation setup is elaborated in section 2. Section 3 demonstrates the investigation of the high-*k* gate dielectric effect on the performance of CL and JL DG-MOSFET based complementary metal oxide semiconductor (CMOS) inverter. Finally, section 4 concludes the work.

MATERIALS AND METHODS

The conventional (CL) and junctionless (JL) n/p-type DG-MOSFET structure is depicted in Fig. 1(a) and 1 (b) respectively. A 2D Sentaurus TCAD mixed-mode simulator [17] is picked for the simulation of double gate metal oxide semiconductor field effect transistor (DG-MOSFET). DG-MOSFET is simulated at a fixed channel length (L_g) and interfacial layer thickness (T_i) of 30 nm and 0.2 nm respectively [18]. The Source/Drain doping concentration is set at 10^{20} cm^{-3} and 10^{19} cm^{-3} respectively for CL-DG-MOSFET and JL-DG-MOSFET with arsenic/boron for n-type/p-type. The channel region is doped with boron/arsenic for n-type/p-type at 10^{16} cm^{-3} in the case of CL-DG-MOSFET whereas it is doped with arsenic/boron for n-type/p-type at 10^{19} cm^{-3} in the case of JL-DG-MOSFET [18-19].

The titanium oxide (TiO_2) is used as a high-*k* dielectric (*k* = 40) for gate oxide to investigate the effect of the same on the performance of complementary metal oxide semiconductor (CMOS) inverter [18]. The effective oxide thickness (EOT) is set at 1 nm throughout the study [19]. The physical thickness (T_{Phy}) for the TiO_2 is calculated as per $T_{Phy} = \{(EOT - T_i) \times k/3.9\}$.

The parameters used for simulating the DG-MOSFET devices are tabularized in Table 1. Further, the Metal gate having a work function of 4.6 eV & 4.8 eV is utilized to dodge the poly-depletion effects in CL-DG-MOSFET and JL-DG-MOSFET respectively [18-19]. The saturation velocity (V_{Sat}) is set at 2.036×10^7 cm/s for the correct coupling of the carrier's transport phenomena [20-23]. The simulation study is performed by including the Philip unified and Lombardi mobility models, band to band auger recombination along with SRH recombination/generation model, and MLDA quantization model [17, 21]. Further, the $I_D - V_{gs}$ characteristics of n/p – type CL-DG-MOSFET & JL-DG-MOSFET is in good calibration with the data presented in s and is reproduced as presented in Fig. 1 (c) & Fig. 1 (d) respectively.

RESULT AND DISCUSSION

It is a renowned matter in semiconductor engineering that the digital behavior of the FET devices changes by changing the SiO_2 with high-*k* dielectrics as gate oxide [25-26]. Nevertheless, the change in digital behavior due to high-*k* gate dielectrics differs from one device to another, and hence in-circuit performances build using these devices too.

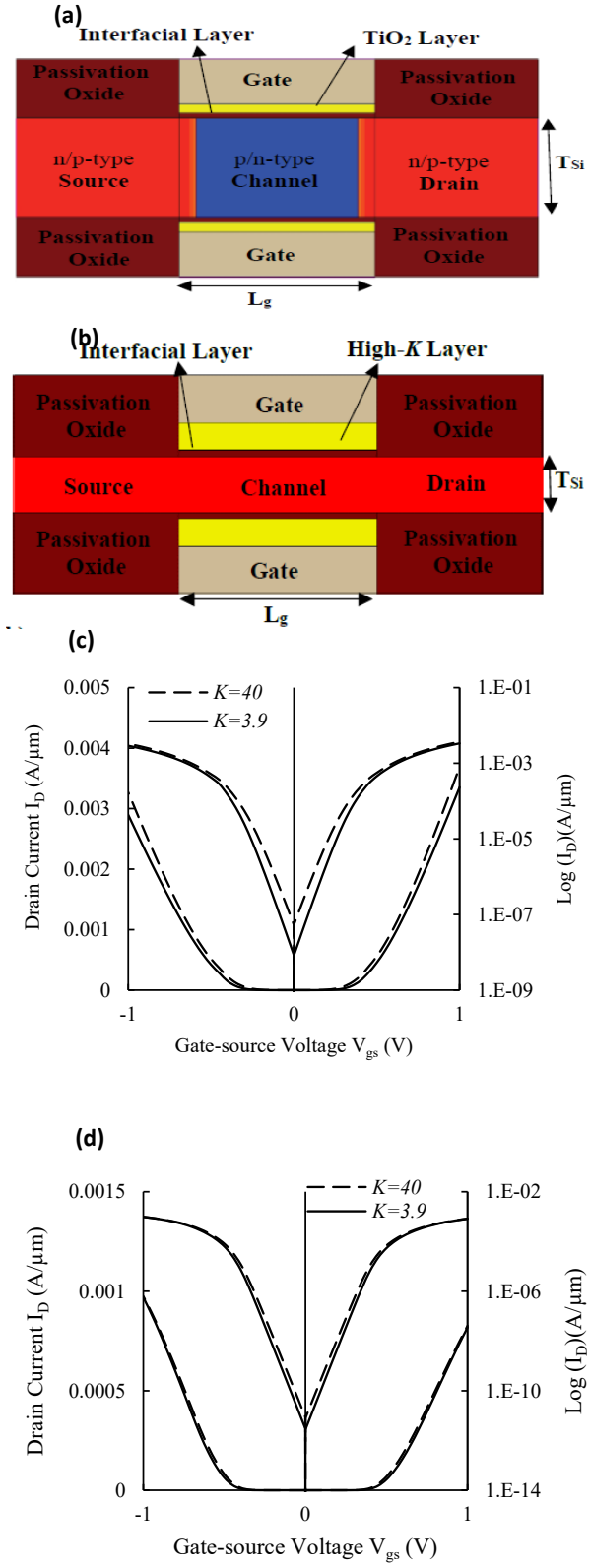

Fig. 1. Schematic view of (a) CL-DG-MOSFET (b) JL-DG-MOSFET & I_D-V_{gs} characteristic of (c) CL-DG-MOSFET (d) JL-DG-MOSFET.

Table 1. DG-MOSFET parameter details.

Parameters	CL-DG-MOSFET	JL-DG-MOSFET
Channel Length (L_g)	30 nm	30 nm
Interfacial Layer Thickness (T_I)	0.2 nm	0.2 nm
EOT	1 nm	1 nm
Channel Thickness (T_{Si})	6-14 nm	6-14 nm
Work function (Φms)	4.6 eV	4.8 eV
Channel Doping	1×10^{16} atoms/cm^{-3}	1×10^{19} atoms/cm^{-3}
Source/Drain Doping	1×10^{20} atoms/cm^{-3}	1×10^{19} atoms/cm^{-3}

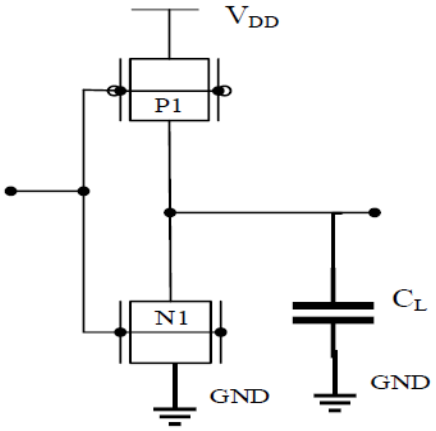

Fig. 2. DG-MOSFET-based CMOS inverter circuit.

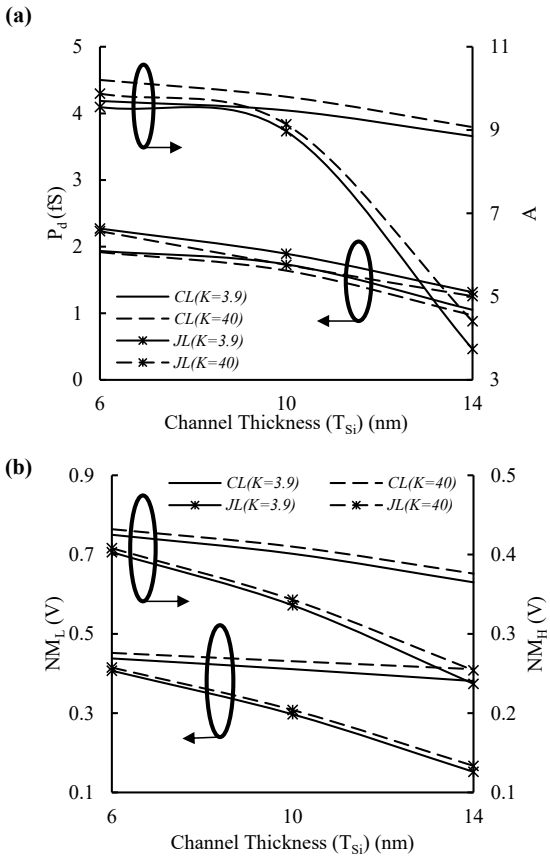

Fig. 3. (a) P_d & A Vs T_{Si} (b) NM_L & NM_H Vs $T_{Si.}$

With this in conception, the effect of high-*k* gate dielectric (in gate-stack (GS) configuration) on the performance of conventional (CL) DG-MOSFET based CMOS inverter and junctionless (JL) DG-MOSFET based CMOS inverter has been investigated in this section. A CMOS inverter is chosen for the investigation as it is one of the fundamental building blocks for most of the digital circuits. A DG-MOSFET based CMOS inverter is presented in Fig. 2.

The speed of a digital circuit is of utmost importance for fast operations. The propagation delay (P_d) of the CMOS inverter quantifies the speed. The smaller the P_d faster will be the operation. Further, the regenerative property is another one that must be possessed by the inverter circuit to ensure that a distributed signal converges back to within the noise margins range after passing through several logical stages. Inverter Gain (A) is the parameter that can be used to quantify the regenerative property [27]. The propagation delay (P_d) and gain (A) of CL-DG-MOSFET based CMOS inverter and JL-DG-MOSFET based CMOS inverter for k = 3.9 (SiO_2) & k = 40 (TiO_2) at the distinct value of channel thickness (T_{Si}) are shown in Fig. 3(a). It is noticed that the propagation delay (P_d) reduces when the high-*k* dielectric is used as a gate oxide in both CL-DG-MOSFET and JL-DG-MOSFET based CMOS inverters. Further, the high-*k* gate dielectric enhances the gain (A) of both CL-DG-MOSFET and JL-DG-MOSFET based CMOS inverters.

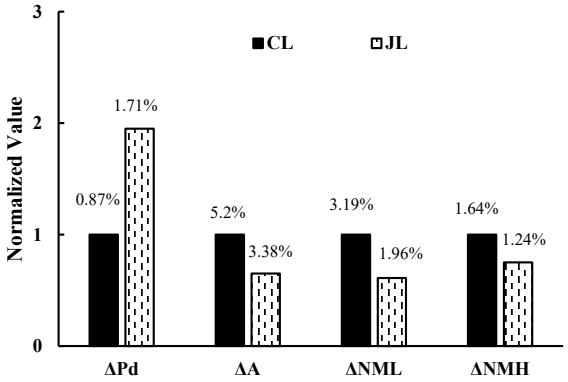

Fig. 4. Comparison of ΔFOMs of conventional and junctionless DG-MOSFET based CMOS inverter.

Further, the reduction in channel thickness (T_{Si}) results in an increase of gain (A) for all the cases but at the cost of an increase in propagation delay. Moreover, it can also be noticed that the CMOS inverter build using CL-DG-MOSFET is having a lower propagation delay (P_d) and high gain (A) as compared to JL-DG-MOSFET based CMOS inverter. Thus, CL-DG-MOSFET based CMOS inverter has high speed and better regenerative properties.

Tewari et al. [28] stated that the noise margins that is, low noise margin (NM_L) and high noise margin (NM_H) are the vital figure of merits to investigate the stability of a CMOS-Inverter. The NM_L and NM_H of CL-DG-MOSFET based CMOS inverter and JL-DG-MOSFET based CMOS inverter for k = 3.9 (SiO_2) & k = 40 (TiO_2) at the distinct value of channel thickness (T_{Si}) are shown in Fig. 3(b). It is found that the usage of high-k dielectric (k = 40) as gate oxide increases the NM_L as well as NM_H in both CL-DG-MOSFET and JL-DG-MOSFET based CMOS inverters. Further, the noise margins and hence stability of CL as well as JL DG-MOSFET based inverters can be improved by scaling down the channel thickness (T_{Si}). It is also noticed that the JL-DG-MOSFET based CMOS inverter has lower NM_L & NM_H and hence stability as compared to CL-DG-MOSFET based CMOS inverter for all values of gate dielectric constant (k).

Furthermore, the change in various figures of merits (FOMs) caused by high-k gate dielectric i.e., ΔFOM (= $|FOM_{(k=3.9)} - FOM_{(k=40)}|$) in CL-DG-MOSFET based CMOS inverter and JL-DG-MOSFET based CMOS inverter are depicted in Fig. 4. It can be realized that change in P_d (ΔP_d) is higher for CMOS inverter build using JL-DG-MOSFET (~39 fS) as compared to build using CL-DG-MOSFET (~ 17 fS). However, the improvement in gain A (ΔA) is approximately 35% higher in CL-DG-MOSFET based CMOS inverter in comparison to JL-DG-MOSFET based CMOS inverter. The ΔNM_L & ΔNM_H are 14 mV & 7 mV respectively in CL-DG-MOSFET based CMOS inverter and are 8 mV & 5 mV respectively in JL-DG-MOSFET based CMOS inverter.

CONCLUSION

The effect of the high-k gate dielectric in the gate-stack configuration on the behavior of conventional (CL) double-gate (DG) MOSFET and junctionless (JL) DG-MOSFET based CMOS inverters has been carried out and compared through comprehensive 2D TCAD simulation. It is perceived that the usage of high-k dielectric (TiO_2) as gate oxide improves the CMOS inverter performance in both the devices i.e. CL-DG-MOSFET & JL-DG-MOSFET. Nevertheless, the improvement in performance of CMOS inverter ($\Delta FOM = FOM_{k=3.9} - FOM_{k=40}$) is different for CL-DG-MOSFET and JL-DG-MOSFET. The enhancement in low noise ($\Delta NM_L = NM_{L(k=3.9)} - NM_{L(k=40)}$), high noise margin ($\Delta NM_H = NM_{H(k=3.9)} - NM_{H(k=40)}$), gain ($\Delta A = A_{(k=3.9)} - A_{(k=40)}$) and propagation delay ($\Delta P_d = P_{d(k=3.9)} - P_{d(k=40)}$) is 14 mV, 7 mV, 0.5 & 17 fS respectively in CL-DG-MOSFET based CMOS inverter whereas it is 8 mV, 5 mV, 0.3 & 39 fS respectively in JL-DG-MOSFET based CMOS inverter. Consequently, it may be adjudged that usage of high-k dielectrics as gate oxide gives superior performance for CMOS inverter build using conventional DG-MOSFET as compared to junctionless DG-MOSFET based inverter.

CONFLICT OF INTEREST

Authors have no conflict of interest.

REFERENCES

[1] Mohapatra N. R., Desai M. P., Narendra S. G., Rao V. R., (2002), The effect of high-K gate dielectrics on deep sub-micrometer CMOS device and circuit performance. *IEEE Trans. Electron Dev*. 49: 826-831.

[2] Zhang W., Fossum J. G., Mathew L., Du Y., (2005), Physical insights regarding design and performance of independent-gate FinFETs. *IEEE Trans. Electron Dev.* 52: 2198-2206.

[3] Tayal S., Nandi A., (2017), Analog/RF performance analysis of channel engineered high-k gate-stack based junctionless trigate-FinFET. *Superlatt. Microst*. 112: 287-295.

[4] Bozorgi Golafzani A., Sedigh Ziabari S., (2020), Representation of a nanoscale heterostructure dual material gate JL-FET with NDR characteristics. *Int. J. Nano. Dimens.* 11: 12-17.

[5] Colinge J. P., Lee C.-W., Afzalian A., Akhavan N. D., Yan R., Ferain I., Razavi P., O'Neill B., Blake A., White M., Kelleher A.-M., McCarthy B., Murphy R., (2010), Nanowire transistors without junctions. *Nat. Nanotechnol.* 5: 225-229.

[6] International Technology Roadmap for Semiconductor (ITRS) for Radio Frequency and Analog/Mixed-signal Technologies, (2013), *www.itrs.net.*

[7] Tayal S., Nandi A., (2017), Analog/RF performance analysis of inner gate engineered junctionless Si nanotube. *Superlatt. Microst*. 111: 862-871.

[8] Momose H. S., Ono M., Yoshitomi T., Ohguro T., Nakamura S. I., Saito M., Iwai H., (1996), 1.5 nm direct-tunneling gate oxide Si MOSFET's. *IEEE Trans. Elect. Dev.* 43: 1233-1242.

[9] Jena B., Dash S., Mishra G. P., (2018), Improved switching speed of a CMOS inverter using work-function modulation engineering. *IEEE Trans. Elect. Dev.* 65: 2422-2429.

[10] Tayal S., Nandi A., (2017), Comparative analysis of high-k gate stack based conventional & junctionless FinFET, in *Proc. of 14th IEEE India Council International Conf. (INDICON)*, 1-4.

[11] Tayal Sh., Samrat P., Keerthi V., Vandana B., Gupta Sh., (2020), Channel thickness dependency of high-k gate dielectric based double-gate CMOS inverter. *Int. J. Nano. Dimens.* 11: 215-221.

[12] Mohapatra S. K., Pradhan K. P., Sahu P. K., (2014), Influence of high-K dielectric on nanoscale DG-MOSFET. *IJAST*. 65: 19-26.

[13] Chowdhury M. H., Mannan M. A., Mahmood S. A., (2010), High-K dielectrics for submicron MOSFETs. *IJETSE*. 2: 8-10.

[14] Prerna M., (2013), Future MOSFET devices using high-k (TiO_2) dielectric. *IJRASET*. 1: 23-28.

[15] Tayal S., Nandi A., (2018), Optimization of gate stack in junctionless Si-nanotube FET for analog/RF applications. *Mater. Sci. Semicond. Proc.* 80: 63-67.

[16] Pradhan K. P., Mohapatra S. K., Sahu P. K., Behera D. K., (2014), Impact of high-K dielectric on analog and RF performance of nanoscale DGMOSFET. *Microelectron. J.* 45: 144-151.

[17] Sentarus Device User Guide. Available: http://www.synopsys.com.

[18] Tayal S., Nandi A., (2018), Effect of high-K gate dielectric in-conjunction with channel parameters on the performance of FinFET based 6T SRAM. *J. Nanoelectron. Optoelec.* 13: 768-774.

[19] Tayal S., Nandi A., (2018), Enhancing the delay performance of junctionless silicon nanotube based 6T SRAM. *Micro Nano Lett.* 13: 965-968.

[20] Granzner R., Polyakov V. M., Schwierz F., Kittler M., Doll T., (2003), On the suitability of DD and HD models for the simulation of nanometer double-gate MOSFETs. *Phys. E.* 19: 33-38.

[21] Tayal S., Nandi A., (2017), Study of 6T SRAM cell using high-k gate dielectric based junctionless silicon nanotube FET. *Superlatt. Microst*. 112: 143-150.

[22] Dixit A., Kottantharayil A., Collaert N., Goodwin M., Jurczak M., Meyer K. D., (2005), Analysis of the parasitic S/D resistance in multiple-gate FETs. *IEEE Trans. Elect. Dev.* 52: 1132-1140.

[23] Nuttinick S., Parvais B., Curatola G., Mercha A., (2007), Double-gate FinFETs as a CMOS technology downscaling option: An RF perspective. *IEEE Trans. Elect. Dev.* 54: 279-283.

[24] Tayal S., Nandi A., (2018), Performance analysis of junctionless DG-MOSFET based 6T SRAM with gate-stack configuration. *Micro Nano Lett.* 13: 838-841.

[25] Tayal S., Nandi A., (2017), Effect of FIBL in-conjunction with channel parameters on analog and RF FOM of FinFET. *Superlatt. Microst*. 105: 152-162.

[26] Tayal S., Nandi A., (2018), Interfacial layer dependence of high-k gate stack based conventional trigate FinFET concerning analog/RF performance, in *Proc. of 4th International Conf. on Devices, Circuits and Systems (ICDCS)*. 305-308.

[27] Rabey J. M., Chandrakasan A. P., Nikolic B., (2003), Digital Integrated Circuits: A Design Perspective, Pearson Education.

[28] Tewari S., Biswas A., Malik A., (2015), Investigation of high-performance CMOS with p-Ge and n-InGaAs MOSFETs for logic applications. *IEEE Trans. Nano.* 14: 275-281.