

A design of improved nanoscale U-Shaped TFET by energy band modification for high performance digital and analog/RF applications

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Abstract

In this study, a new nanoscale U-shaped tunnel field-effect transistor (US TFET) structure is proposed. In order to start the design process, the drain region of the conventional US TFET is divided into two distinct parts with N+ and N- doping which is named the drain doping engineering (DDE). It is considered that the tunneling barrier at the channel-drain junction is increased and consequently the ambipolar current is decreased considerably. To continue the design process, the dual work function (DW) in the DDE-US TFET has been used to ameliorate the DC characteristics and the cutoff frequency. Moreover, we have used the metal implant (MI) in the source-side oxide of DDE-DW-US TFET as a technique to improve the device for high-frequency and low-power applications. The 2-D TCAD simulation results not only indicate the superiority of the proposed structure (DDE-DW-MI-US TFET) compared to others in terms of the high-frequency performance, but also illustrate the improvement of the DC parameters. Finally, the proposed device has been investigated by increasing the length of implanted metal in the source-side oxide. It is found that selecting the appropriate length contributes significantly to improve high-frequency performance.

Keywords: Ambipolar Current; Drain Doping Engineering; Dual Work Function; Metal Implant; Nanoscale U-Shaped Tunnel Field-Effect Transistor (US TFET).

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INTRODUCTION

The continuous scaling of MOSFET dimensions has been improving operating speed, power dissipation, and high-frequency performance. Despite of these advantages, MOSFET scaling has a number of problems [1, 2] such as the short-channel effects, high OFF current, and the subthreshold slope (SS) of over 60 mV/decade [3–6]. These problems lead to decrease in performance of the device in low-power and analog/RF applications [7, 8]. The tunnel field-effect transistor (TFET) was introduced to overcome these problems. TFET provides the subthreshold slope of below 60 mV/decade by relying on band-to-band tunneling (BTBT). Moreover, TFET

was considered as a promising candidate for substitution of MOSFET due to its low off current and its low SS [9], which significantly reduces the short channel effects. So TFETs are appropriate for analog and RF applications [10–13]. Aside from the advantages, TFET suffers from the weak ON current and the high ambipolar current [14–17]. Several methods have been proposed to resolve these two important difficulties, some of which are discussed.

The bandgap engineering is an effective method to improve the ON current and the ambipolar conduction. But this is an expensive solution [18–21]. Gate dielectric engineering is a method that can increase the ON current while reducing the ambipolar current. But this approach exacerbates

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the parasitic capacitances and undermines the high-frequency performance [22]. The gate-drain overlap is another solution to suppress the ambipolar current [23, 24], but similar to the previous one, this method also endangers high-frequency performance by increasing the gate-to-drain capacitance (C_{gd}) [25]. Moreover, light doping in the drain region has been proposed to suppress the ambipolar current [26, 27]. However, this technique produces a low drive current as a result of increasing the contact resistance [28].

Several new nanoscale TFET structures have been proposed to improve the device performance. L-shape TFET and U-shape TFET are suitable for improving I_{on} . Due to the recessed gate on the substrate, tunneling regions in both structures are expanded and so the ON currents are improved [29, 30]. A symmetric U-shaped gate TFET (SUTFET) has been recently introduced to improve the DC characteristics [31]. However, the performance of the structure has not been analyzed for RF parameters. Overall, it is concluded that most of the introduced methods lead to weaken the high-frequency performance and the ON current. Also, a number of them have not been studied in this regard. Accordingly, we introduce a new nanoscale U-shaped TFET (US TFET) that it has the enhanced high-frequency performance, the improved ON current and suppressed ambipolar behavior. The first solution is to establish two differently-doped regions (N^+ and N^-) at the drain. Even though the drain doping engineering (DDE) approach [32] effectively reduces the ambipolar current, it has little impact on RF parameters and does not change the ON current. Therefore, two other solutions have been offered to ameliorate the ON current and high-frequency performance. We have used the dual work function (DW) at the US gate, which narrows the tunneling barrier at the source-channel junction and so promotes the ON current. This solution is also effective for improving the ambipolar current and high-frequency performance of the device. In an attempt to achieve more improvement of the DC characteristics and high-frequency parameters, the metal implant (MI) has been proposed and investigated. This idea has already been introduced in the literature [21, 33, 34]. In our work, the metal strip has been implanted in the source-side oxide. It causes to enhance the ON current and remarkably the cutoff frequency.

The rest of this paper is structured as follows. In

Section 2, the device structure, simulation setup, and possible fabrication process are discussed. In Section 3, we have compared the proposed structure with others in terms of the ambipolar current, the DC characteristics, and the high-frequency performance and then investigated the effects of length and thickness of implanted metal in the proposed structure. Finally, Section 4 presents the conclusions.

EXPERIMENTAL SECTION

Device Structure and Simulation Setup

Fig. 1(a-d) shows the schematic representations of conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET (the proposed structure). All simulations were carried out using Silvaco- Atlas device simulator. The nonlocal BTBT model was used for transverse tunneling. Fig. 2 depicts the calibrated model based on the reported results in [35], which has already been calibrated using the experimental results in [36]. In this simulation, the Lombardi mobility (CVT) model has been used to study the effects of temperature, impurity concentration, and transverse fields. Furthermore, the Shockley-Read Hall (SRH) recombination model, the Auger recombination model, the bandgap narrowing (BGN) model, the Fermi-Dirac model, and the Drift-Diffusion current model have been used.

The P^+ source and the N^+ drain regions doping concentrations are assumed to be $1 \times 10^{20} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, respectively. The P^- channel and the N^- drain regions doping concentrations are assumed to be $1 \times 10^{17} \text{ cm}^{-3}$. All the structures are silicon-based. The thickness of the buried oxide layer (SiO_2) is 20 nm. Further, HfO_2 is selected for the dielectric material at the US gate to enhance the ON current. Other parameters are listed in Table 1.

The possible steps of fabricating the proposed DDE-DW-MI-US TFET are briefly explained as follows.

- The Si- source, channel, and drain regions are deposited by epitaxial growth. Then, the excess Si is etched and a layer of HfO_2 is deposited. The deposition of high-k gate oxide can be conducted utilizing the physical vapor deposition method. This technique causes a layer of HfO_2 without the formation of low-k interfacial layer [37].

- The doping of the drain region could be performed by heavy and light energy implants to get the needed doping profile in the drain region. The exact drain doping is possible through rapid annealing following a small diffusion coefficient of

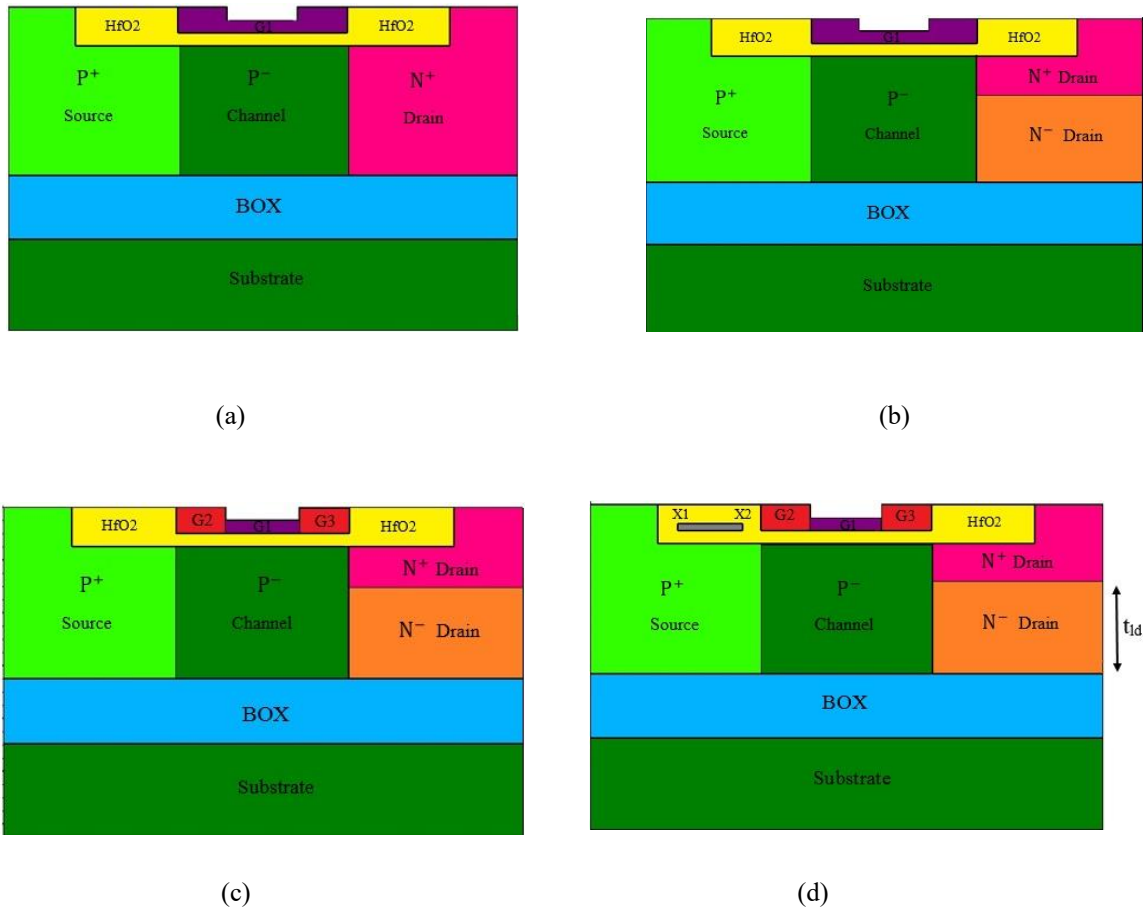


Fig. 1. Cross-sectional view of (a) conventional US TFET, (b) DDE-US TFET, (c) DDE-DW-US TFET, and (d) DDE-DW-MI-US TFET (proposed structure).

Table 1. Device design parameters.

Parameters	value
Channel length	50 nm
Drain and source lengths	50 nm
Thickness of the N ⁻ drain (t_{id})	7 nm
Thickness of channel	10 nm
Thickness of silicon body	13 nm
Lengths of G2 and G3	15 nm
Length of MI	20 nm
Thickness of G1	1 nm
Thicknesses of G2 and G3	2 nm
Thickness of MI	0.5 nm
Work function of G1	4.6 eV
Work functions of G2 and G3	4.3 eV
Work function of MI	5.9 eV

dopant [38].

- Varying the amount of nitrogen over the single gate material may help to form a dual work function

[39].

- The metal implant in the source-side oxide is possible through the ALD (atomic layer deposition)

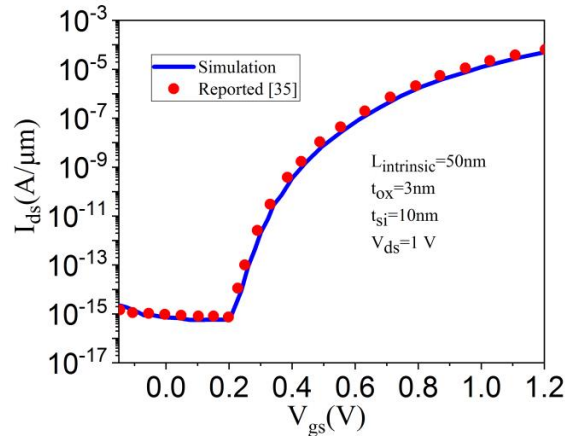


Fig. 2. $I_{ds} - V_{gs}$ calibration from the result reported in [35].

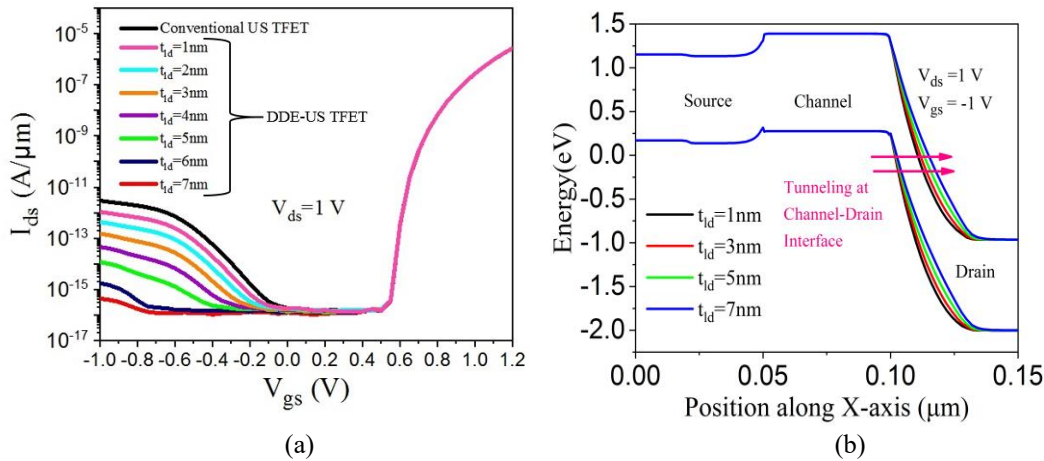


Fig. 3. (a) Transfer characteristics for conventional US TFET and DDE-US TFET with different light-doped drain region thicknesses (t_{id}) (b) Energy band diagram of DDE-US TFET for various values of t_{id} in the ambipolar state.

procedure. The ALD technique is applied for depositing diverse thin films through the vapor phase. A tunable film composition could be formed by controlling the thickness at Angstrom level [40]. The procedures occur under modest temperature. Considering this procedure, we have assumed the thickness of the metal to be 0.5 nm which might be simply obtained through the ALD process. Therefore, the ALD method can be used to deposit Hf, Cu, Au, and Pt. [41]. Moreover, low chemical vapor is beneficial for depositing thin-film layers [42].

RESULTS AND DISCUSSION

Drain Doping Engineering for Ambipolar Current Suppression

First of all, we use drain doping engineering

(DDE) and create the DDE-US TFET with differently-doped regions (N^+ and N^-) at the drain. Fig. 3(a) shows a comparison between the transfer characteristics of conventional US TFET and DDE-US TFET with N^- drain region thickness (t_{id}) variation. Obviously, due to divide the drain into two distinct regions with N^+ and N^- doping, the ambipolar current is considerably reduced compared to a conventional US TFET. The presence of N^+ drain region is to ensure the ohmic contact with the electrode of the drain [32]. Increasing the thickness of the N^- drain region (t_{id}) from 1 nm to 7 nm helps to reduce the ambipolar current. So, the ambipolar current is depended on the thickness of the light-doped drain region (t_{id}). However, variation of t_{id} does not change the ON current. Fig. 3(b) shows

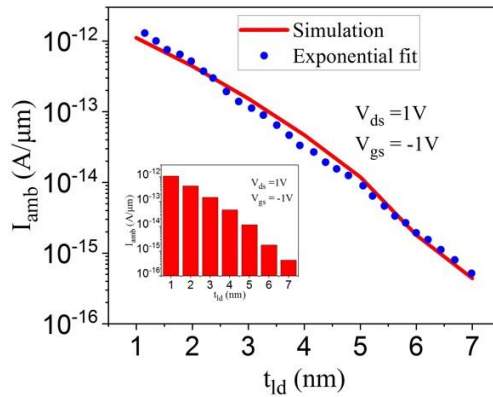


Fig. 4. I_{amb} against t_{ld} for DDE-US TFET, fitted with an exponential function.

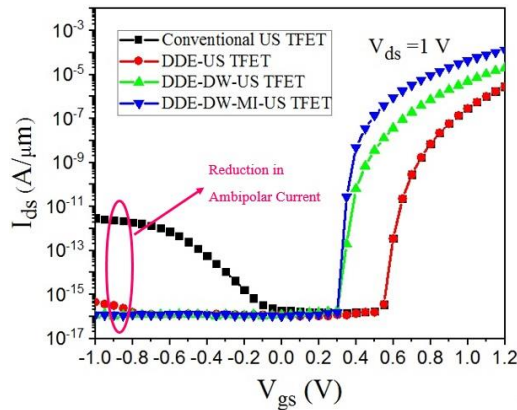


Fig. 5. Transfer characteristics for conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET.

the energy band diagram of the DDE-US TFET for various values of t_{ld} in the ambipolar state. The tunneling barrier at the channel-drain interface is gradually increased by increasing the thickness of the light-doped drain region. It decreases the tunneling rate and consequently, suppresses the ambipolar current. In this work, the thickness of the N⁻ drain region (t_{ld}) is assumed at 7 nm with a very low I_{amb} of 4.54×10^{-16} A/ μ m. For t_{ld} = 7 nm, the ambipolar current is almost eliminated up to $V_{gs} = -0.7$ V. Fig. 4 illustrates the variation of I_{amb} for the different values of t_{ld} , fitted by an exponential function of the following form.

$$I_{amb} = (6 \times 10^{-12}) \times e^{-1.346t_{ld}}$$

Effects of Dual Work Function and Metal Implant on DC characteristics

As evident from Fig. 3(a), conventional US TFET and DDE-US TFET structures have a similar ON current

(I_{on}). Therefore, the drain doping engineering is not effective on the ON current and other solutions have to propose in order to improve I_{on} . The first solution is to use the dual work function (DW) at the US gate. For this purpose, the US gate has been separated into three segments, named G1, G2, and G3. The middle gate (G1) work function has been assumed 4.6 eV. A work function of 4.3 eV has been also assumed for both source-side (G2) and drain-side (G3) gates. This designed device is named DDE-DW-US TFET. The smaller work function at the source-side gate (G2) increases I_{on} while the smaller work function at the drain-side gate (G3) limits the ambipolar conduction. The second solution for more improving the ON current is the metal implant (MI) in the source-side oxide of the previous structure which is named DDE-DW-MI-US TFET. It increases the tunneling area at the source-channel boundary.

Fig. 5 shows the transfer characteristics of conventional US TFET, DDE-US TFET, DDE-DW-

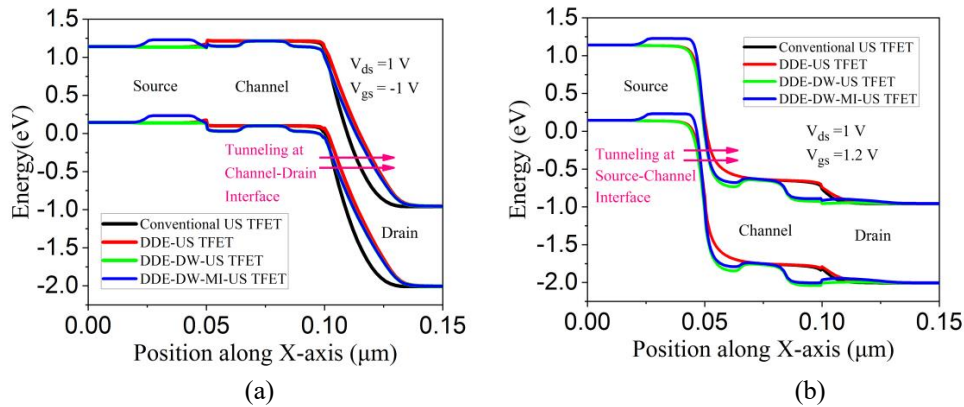


Fig. 6. Energy band diagram (a) ambipolar state (b) ON state for conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET along a cutline 1 nm below HfO_2 -Si interface.

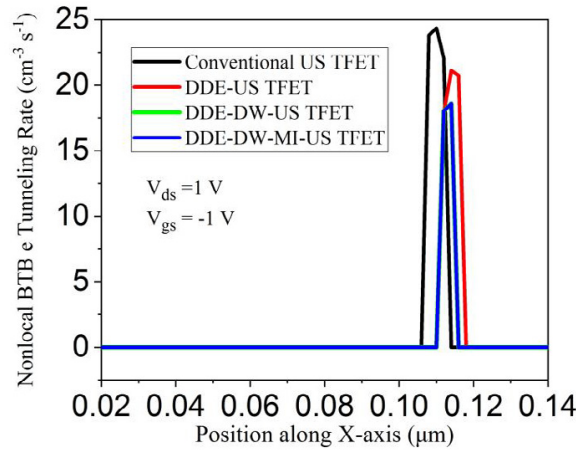


Fig. 7. Nonlocal BTB electron tunneling rate for conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET.

US TFET, and DDE-DW-MI-US TFET. It is obvious that use of the dual work function of the US gate improves the device performance in terms of ON current and ambipolar behavior. For a deep physical understanding of the effect of dual work function in the ambipolar state, the energy band diagrams of the four structures are presented in Fig. 6(a). As can be seen in this figure, due to the smaller work function at the drain-side gate (G3), the DDE-DW-US TFET and DDE-DW-MI-US TFET have broader tunneling barrier at the drain-channel interface compared to DDE-US TFET. It causes to suppress the ambipolar current. Accordingly, as illustrated in Fig. 5, the ambipolar current can be eliminated for $V_{gs} < -0.7$ V due to the dual work function. When I_{amb} falls below the OFF current, it can say that the ambipolar current

is eliminated [43]. Fig. 7 illustrates the nonlocal BTB electron tunneling rate in the ambipolar state ($V_{gs} = -1$ V and $V_{ds} = 1$ V) for the four structures. As shown in this figure, the electron tunneling rate in DDE-DW-US TFET and DDE-DW-MI-US TFET is less due to the use of the combination of the two ideas DDE and DW, which indicates a decrease in the ambipolar current.

Fig. 6(b) shows the energy band diagram for the four structures at ($V_{gs} = 1.2$ V and $V_{ds} = 1$ V) in the ON state. Using the smaller work function for the source-side gate (G2) provides a smaller tunneling barrier length at the source-channel interface. Further, the metal implant (MI) in the source-side oxide increases the energy band level in the source region, which also helps to reduce the barrier length. Thus, the combination of these

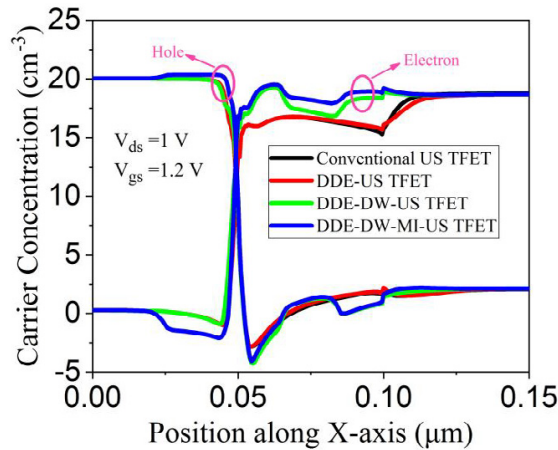


Fig. 8. Comparison of carrier concentration for conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET.

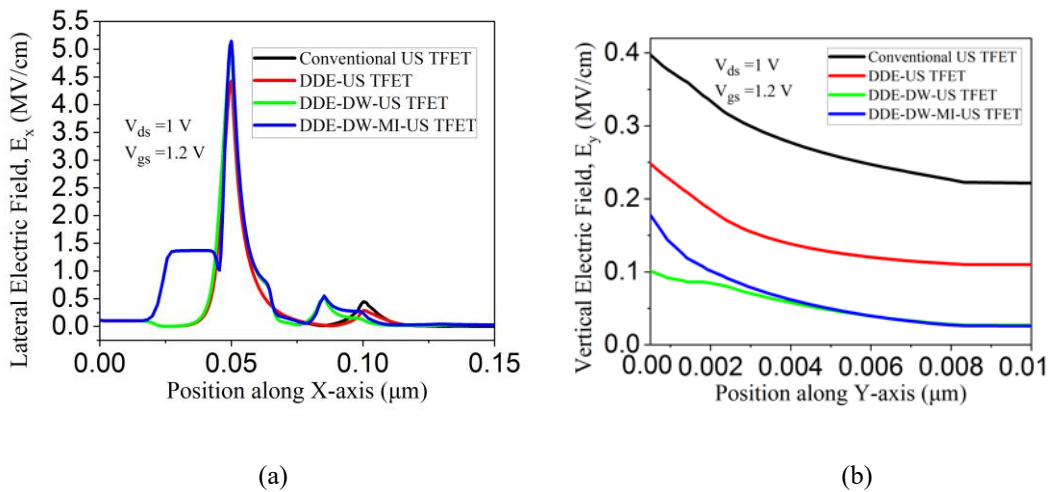


Fig. 9. Comparison of (a) Lateral electric field (E_x) (b) Vertical electric field (E_y) for conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET.

two approaches makes the narrowest tunneling barrier in the source-channel interface for DDE-DW-MI-US TFET. As shown in Fig. 5, this device has the highest I_{on} . Furthermore, Fig. 5 indicates that DDE-DW-MI-US TFET has the lowest threshold voltage (V_{th}). Here, V_{th} is the same V_{gs} obtained from the current characteristic curve, where $I_{ds} = 6.43 \times 10^{-8} \text{ A}/\mu\text{m}$.

The ON current improvement is better analyzed in Fig. 8 by plotting the carrier concentrations of the four structures. This figure illustrates that the DDE-DW-MI-US TFET has the highest electron concentration in the channel region. The simultaneous effects of dual work function of the US gate and metal implant in the source-side oxide increase the overlap between the valence band of the source and the conduction

band of the channel. Therefore, as shown in Fig. 6(b), potential barrier has reduction at the source-channel junction and this can increase tunneling rate at the same junction.

Moreover, Fig. 9(a) shows the variation of lateral electric field (E_x) for the four structures in the ON state. As shown in Fig 9(a), four of the structures have electrical field peaks in the source-channel junction. However, the electric field peaks of DDE-DW-US TFET and DDE-DW-MI-US TFET are more than others, due to the use of the smaller work function at the source-side gate (G2), which makes a shorter tunneling barrier and so promotes electron transport from the source to the channel. The electric field peak of the DDE-DW-MI-US TFET is higher which is indicating a stronger electric field. This outcome can be attributed to

Table 2. Comparison between conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET.

Parameter	Conventional US TFET	DDE-US TFET	DDE-DW-US TFET	DDE-DW-MI-US TFET
I_{on} (A/ μm)	2.85×10^{-6}	2.85×10^{-6}	2.04×10^{-5}	1.33×10^{-4}
I_{off} (A/ μm)	1.89×10^{-16}	1.18×10^{-16}	1.17×10^{-16}	1.11×10^{-16}
I_{on}/I_{off}	1.51×10^{10}	2.41×10^{10}	1.74×10^{11}	1.20×10^{12}
I_{amb} (A/ μm)	3.02×10^{-12}	4.54×10^{-16}	1.13×10^{-16}	1.15×10^{-16}
V_{th} (V)	0.57	0.57	0.52	0.47
SS (mV/dec)	16.75	16.73	16.53	9.48

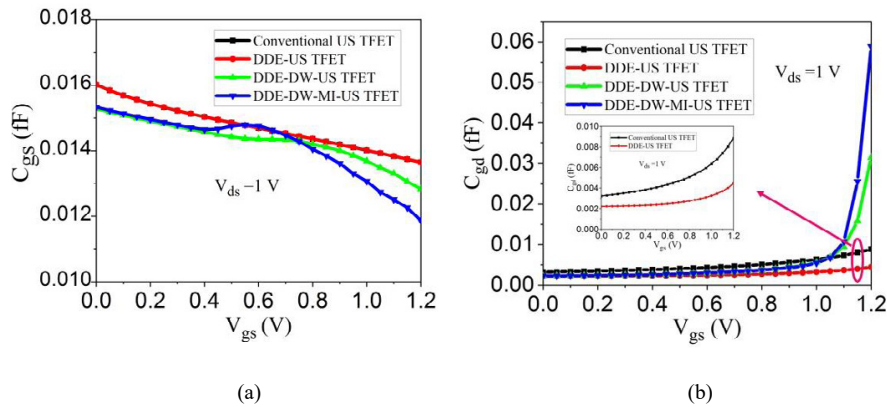


Fig. 10. Comparison of (a) gate-to-source capacitance (b) gate-to-drain capacitance for conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET.

metal implant in the source-side oxide, which cause to achieve the highest electron tunneling at the S/C junction. Selecting the proper work function for the implanted metal also contributes to this phenomenon. On the other hand, due to the using smaller work function at the drain-side gate (G3), two additional peaks appear in the channel region near the drain. Fig 9(b) shows that the vertical electric field (E_y) at the drain-channel junction for DDE-DW-US TFET and DDE-DW-MI-US TFET is reduced compared to other structures. The decrease in electric field at the drain-channel boundary is due to the smaller work function at the drain-side gate (G3). So the DDE-DW-US and DDE-DW-MI-US TFET have higher reliability. Because increasing the y-direction electric field at the drain-channel boundary increases the kinetic energy of the electrons and consequently, it can endanger the gate oxide.

A comparison between conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET is presented in Table 2. The DDE-DW-MI-US TFET has the best performance in terms of I_{on} , I_{off} , I_{on}/I_{off} , V_{th} and SS compared to other structures. Moreover, the DDE-DW-MI-US

TFET has a very low I_{amb} . It is noticeable that Ref. [44] clarifies that the dimensions of its proposed device are in accordance with ITRS requirements. The dimension of our proposed structure channel length is similar to the one structure of Ref. [44].

Comparing the Performance of High-Frequency of DDE-DW-MI-US TFET With Other Structures

The gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances are plotted for all structures in Fig. 10(a) and (b). Increasing the parasitic capacitance is not favorable for the AC applications of the device. Therefore, reducing C_{gs} and C_{gd} improve the RF performance [45]. According to Fig. 10(a), the proposed structure has the least C_{gs} for $V_{gs} > 0.75$ V due to the reduction in the potential barriers in the source-channel interface. This can be attributed to the smaller work function at the source-side gate (G2) and metal implant in the source-side oxide. In addition, the minimum C_{gs} provides the maximum gate control over the channel. Meanwhile, Fig. 10 (b) shows that the C_{gd} remains relatively unchanged in different structures up to $V_{gs} = 1$ V. Only for $V_{gs} > 1$ V, the C_{gd} is increased due to the reduction in the potential

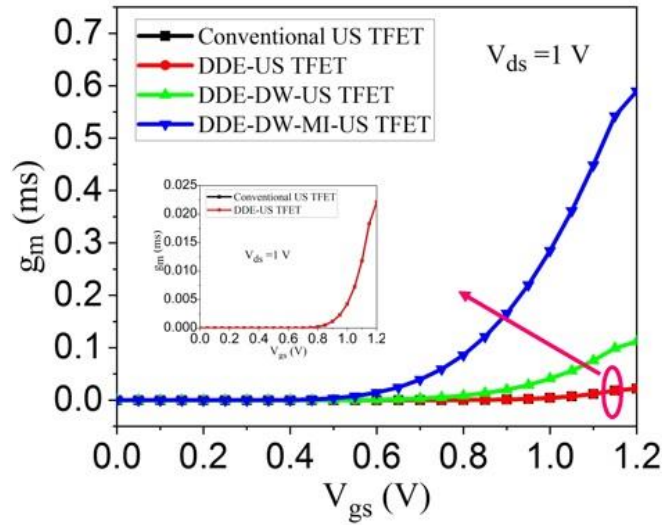


Fig. 11. Comparison of transconductance for conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET.

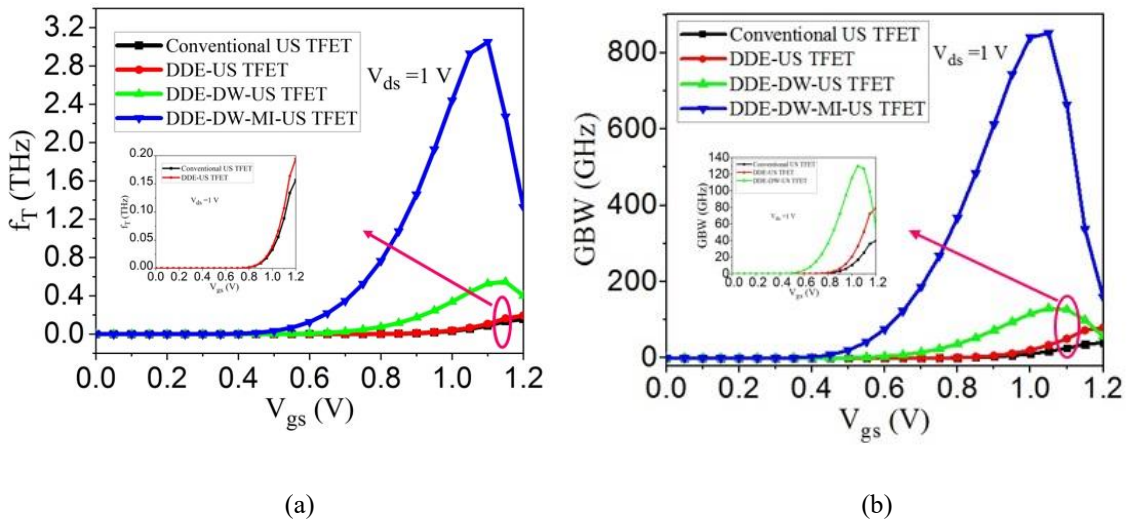


Fig. 12. Comparison of (a) cut-off frequency (b) gain-bandwidth product for conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET.

barriers at the channel-drain junction and the formation of the inversion layer from the drain region towards the source region. Increasing C_{gd} can be attributed to the smaller work function at the drain-side gate (G3) and implanted metal in the source-side oxide. Moreover, transconductance (g_m) is also an important parameter in high-frequency applications [46]. Fig. 11 shows the g_m in different structures. The considerable rise of g_m is obvious in the DDE-DW-MI-US TFET compared to the other three structures, which is due to the simultaneous effects of dual work function of the

US gate and implanted metal in the source-side oxide. As mentioned, the combination of these two ideas expands the tunneling region (S/C), which boosts I_{on} and accordingly increases the g_m in DDE-DW-MI-US TFET.

The cutoff frequency (f_T) is also an essential parameter in evaluating the device for RF applications and is calculated as follows [47].

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Fig. 12(a) illustrates the variation of the cutoff

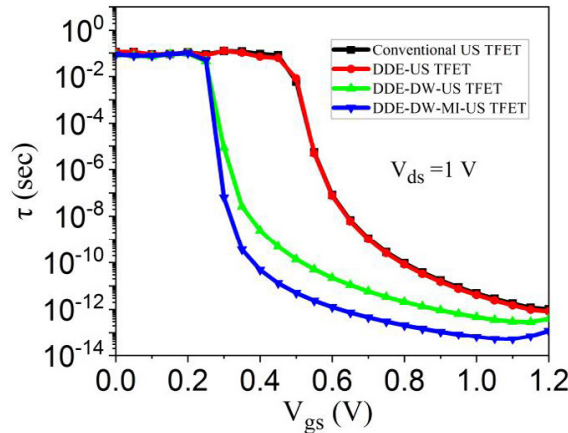


Fig. 13. Comparison of transit time for conventional US TFET, DDE-US TFET, DDE-DW-US TFET, and DDE-DW-MI-US TFET.

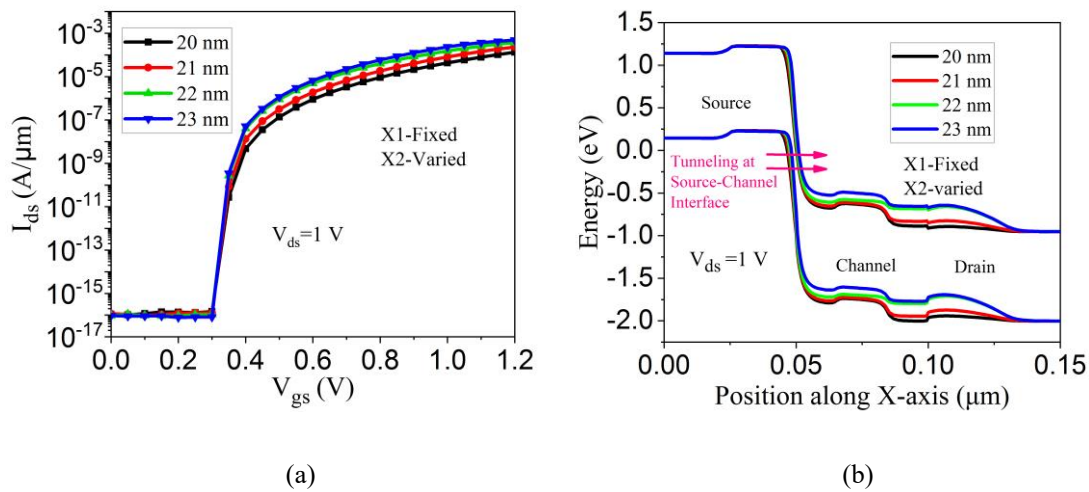


Fig. 14. Comparison of (a) I_{ds} versus V_{gs} curve (b) energy band diagram under ON state for the DDE-DW-MI-US TFET with shift in X2 position.

frequency for all structures. The DDE-DW-MI-US TFET provides the higher f_T at lower gate bias due to the higher g_m [48] and the lower C_{gs} and after that, it falls due to an increase in C_{gd} .

Another critical parameter regarding the high-frequency performance is the gain-bandwidth product (GBW) calculated as follows [49].

$$GBW = \frac{g_m}{20\pi(C_{gd})}$$

Fig. 12 (b) depicts the GBW for all structures. The DDE-TDW-MI-US TFET has the highest GBW due to the considerable rise of g_m . Similar to the f_T , the GBW also is improved with the increase in gate-source voltage to peak and after that, it falls due to the rising C_{gd} .

Transit time (τ), another significant parameter

for evaluating the device speed, which is calculated from the equation below [50].

$$\tau = \frac{1}{2\pi f_T}$$

The τ is the time needed for carriers to transport from source to drain region. Fig. 13 indicates the variations of τ versus gate-source voltage for the four structures. According to the figure, the DDE-DW-MI-US TFET has the smallest τ . Consequently, it is an appropriate candidate for high-speed applications in comparison with the other structures.

Effects of the Implanted Metal Length and Thickness on Proposed DDE-DW-MI-US TFET

In this section, the effect of the length of the

Table 3. Obtained DC parameters of the DDE-DW-MI-US TFET with shift in X2 position.

Length of metal implant (nm)	I_{on} (A/ μm)	I_{off} (A/ μm)	I_{on}/I_{off}	I_{amb} (A/ μm)	V_{th} (V)	SS (mV/dec)
20	1.33×10^{-4}	1.11×10^{-16}	1.20×10^{12}	1.15×10^{-16}	0.47	9.48
21	2.31×10^{-4}	1.11×10^{-16}	2.08×10^{12}	1.15×10^{-16}	0.45	8.59
22	3.68×10^{-4}	1.11×10^{-16}	3.31×10^{12}	1.15×10^{-16}	0.38	7.87
23	4.86×10^{-4}	1.11×10^{-16}	4.38×10^{12}	1.15×10^{-16}	0.31	7.62

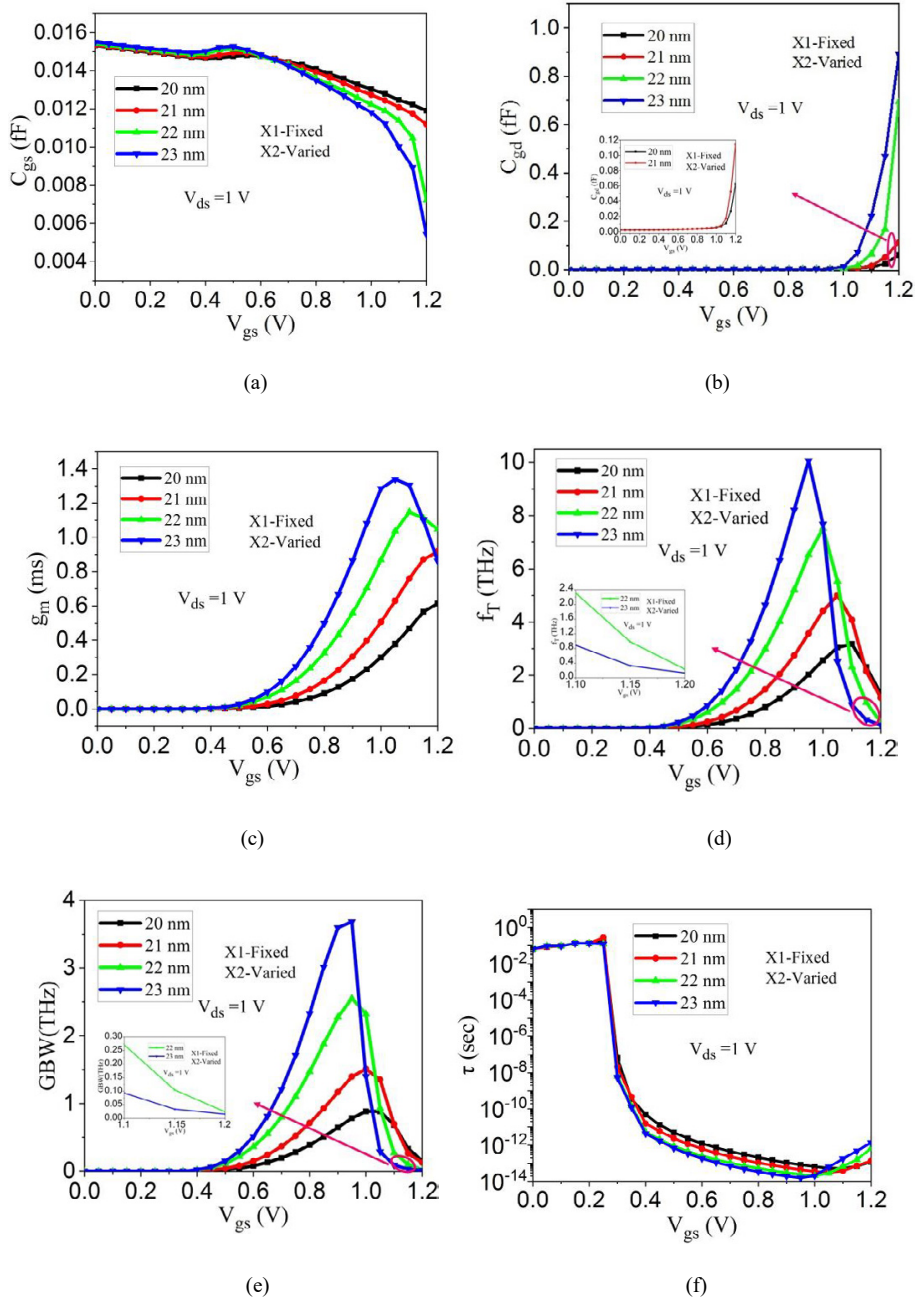


Fig. 15. High frequency Performance of the DDE-DW-MI-US TFET with shift in X2 position. (a) gate-to-source capacitance (b) gate-to-drain capacitance (c) transconductance (d) cut-off frequency (e) gain-bandwidth product (f) transit time.

Table 4. Obtained dc parameters of the proposed DDE-DW-MI-US TFET for different thickness of implanted metal in the source-side oxide.

Thickness of metal implant (nm)	I_{on} (A/ μm)	I_{off} (A/ μm)	I_{on}/I_{off}	I_{amb} (A/ μm)	V_{th} (V)	SS (mV/dec)
0.5	1.33×10^{-4}	1.11×10^{-16}	1.20×10^{12}	1.15×10^{-16}	0.47	9.48
0.75	1.34×10^{-4}	1.11×10^{-16}	1.21×10^{12}	1.15×10^{-16}	0.47	9.38
1	1.4×10^{-4}	1.11×10^{-16}	1.26×10^{12}	1.15×10^{-16}	0.47	8.82

implanted metal on the DC performance of DDE-DW-MI-US TFET is investigated. For this purpose, four lengths (namely 20, 21, 22, and 23 nm) have been considered. It is obvious that extending the metal strip to the left does not change the performance of the DDE-DW-MI-US TFET. Only the case of fixed X1 and varying X2 is effective on the proposed structure. Fig. 14(a) shows that extending the metal strip to the right increases the ON current due to the smaller tunneling barrier, which is represented in Fig. 14(b). The DC parameters of DDE-DW-MI-US TFET are presented in Table 3 for different metal implant lengths, in the case of fixed X1 and variable X2. As expected, increasing the length of the implanted metal has no effect on the OFF current and the ambipolar behavior. Next, high-frequency parameters have been studied for the case fixed X1 and variable X2. Fig. 15 (a) and (b) show that the C_{gs} and C_{gd} for different metal lengths. Extending the length of the implanted metal to the right reduces C_{gs} for $V_{gs} > 0.75$ V, whereas C_{gd} remains relatively unchanged up to $V_{gs} = 1$ V and increases only beyond that voltage.

It is clear from Fig. 15(c) that the g_m is increased by using a longer metal strip. Furthermore, it is obvious from the Fig. 15(d) and (e) that by increasing the length of the implanted metal to 23 nm, the f_T and GBW are maximized at $V_{gs} = 0.95$ V. However, due to the higher C_{gd} , the smallest f_T and GBW are obtained at 23 nm for gate-source voltages of over 1.05 V. Considering the inverse relationship between τ and f_T , extending the metal strip to the right reduces τ up to $V_{gs} = 1.05$ V. Only for $V_{gs} > 1.05$ V, τ is increased due to the reduction of f_T . The dependency of τ on the V_{gs} is presented in Fig. 15(f). Moreover, the effect of the implanted metal thickness has been also investigated for 0.5, 0.75, and 1.0 nm. Table 4 shows that changing the thickness does not make much difference in the performance of DDE-DW-MI-US TFET. According

to the literature [21, 33, 34], we consider the thickness of 0.5 nm for the metal.

CONCLUSION

A novel nanoscale US TFET structure (DDE-DW-MI-US TFET) was proposed and investigated. At first, the ambipolar current was suppressed using drain doping engineering by creating two distinct regions with N^+ and N^- doping in the drain. Then, dual work function of gate improved the ON current and ambipolar behavior by the use of the small work function for both source-side and drain-side gates. Next, metal implant in the source-side oxide narrowed the tunneling width at the source-channel interface. This width decreasing helped to improve the ON current. It is illustrated that our proposed structure has the best performance for high-frequency and low-power applications. Also, selecting the appropriate length for the implanted metal improved the high frequency performance of the DDE-DW-MI-US TFET.

CONFLICT OF INTEREST

Authors have no conflict of interest.

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