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SHORT COMMUNICATION

Design, simulation and analysis of high-*K* gate dielectric FinField effect transistor

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Abstract

The devices with additional gates like Fin Field effect transistor (FinFET) provide higher control on subthreshold parameters and are favorable for Ultra large-scale integration. Also, these structures provide high control on current through the channel and with minimum leakage. In this paper we designed a FinFET with high-K gate dielectric material i.e Hafnium oxide as gate oxide. A comparison of similar sized transistor with Air and Silicon dioxide as gate material is performed. The comparison is mainly in terms of performance parameters like transconductance, subthreshold slope, and drain current characteristics. There is an increase in ON current on using a high-K dielectric material and subsequently an improvement in other parameters like subthreshold slope, transconductance and intrinsic gain.

Keywords: *FinFET; Hafnium Oxide; High-K Dielectric; Subthreshold Slope; Transconductance.*

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INTRODUCTION

Fin Field effect transistors (FinFETs) have become successors of Metal oxide semiconductor Field effect transistors (MOSFETs) as they have shown alarming obstacles in nanometer scale. With the existence of two/three gates these FinFETs are found to drive short channel effects (SCE) like Subthreshold slope, drain induced barrier lowering (DIBL) and Subthreshold swinginabetterwaythanplanarMOSFETs.Thishelpsinenablingscalingoftransistor at nanometer technologyregimes.

Over the decades the persistent scaling of MOSFET shas resulted in intensifying of IC sand transistor density. This scaling in nanometer level is tough due to high leakage current [1-3]. The drain voltage starts to influence the channel region in scaled MOSFETs and this causes the gate to lose the channel control. Because of which thebarrier from source to drain is reduced and is termed as Drain induced barrier lowering. This is a serious concern as we go down in technology nodes [2]. This scaling and DIBL causes increase in leakage current between source and drain. Use of high-*K* dielectric materials solves this issue by making the capacitance between channel and gate higher [3].

The thin gate oxides also solve this problem but these thin gate oxides are restricted in gate leakage. Multigate (two/three) FETs have demonstrated as substituteto traditional MOSFETs [4-6]. Extra gate(s) on channel made

transmission of drain voltage from channel.

These extra gates are made to achieve high capacitance across channel and gate. The sequalities made multi gate FETs efficient than MOSFET sw.r.t SCE. Of all Multigate FETs, FinFETs are found to be better substitute to MOSFETs because of its non-complex structure and fabrication [7-10].

In this paper, the simulation and analysis of FinFET is carried out. The I_D VS V_{GS}, subthreshold

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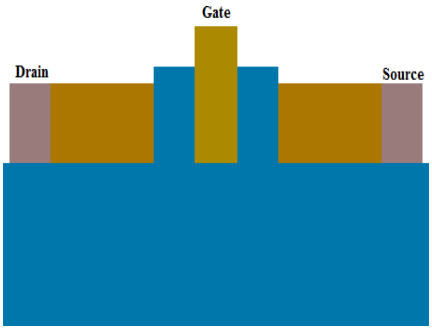

Fig. 1. 3-Dimensional viewof proposed FinFET.

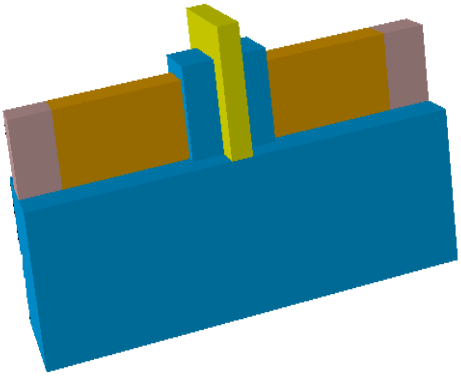

Fig. 2. Front view of proposed FinFET.

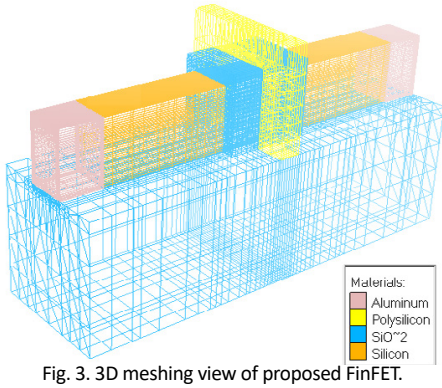

Fig. 3. 3D meshing view of proposed FinFET.

Fig. 4. Top view of proposed FinFET.

slope (SS), transconductance (g_m) characteristics of FinFET for two different materials is found. A high-K dielectric material is also used to find I_DVS V_{GS}characteristics and leakage currents.

THE PROPOSED STRUCTURE OF FINFET

The first delineated FinFET structure is a fully depleted lean channel transistor. With the advent of short channel, the FinFETs have attracted the industry. The channel in MOSFET is horizontal whereas in case of FinFET it is vertical [11]. Therefore, the height of channel decides the width of FinFET. This is the notable property of FinFET termed as Quantization of width [12].

Beyond 1.2nm as oxide thickness is shrinked in order to have performance metrics with control on short channel effects, the silicondioxide tend to lose its dielectric properties. Hence anew dielectric material is needed to avoid electrons tunneling. Thus, a material with higher dielectric constant than SiO_2 is needed. It is observed that the high-*K* dielectric materials reduce OFF current but they include the problem of trapped charges. Thus for the proper control on short channel effects without losing the dielectric properties and to avoid problem of trapped charges HfO_2 is suited as best high-*K* gate dielectric. The corresponding Dielectric constants of materials used are shown in Table.1. With reference to Equivalent oxide thickness, a high-*K* material stores increased charge [13, 14]. This is because of increase in capacitance. As the capacitance is proportional directly to materials dielectric constant, increase in dielectric constant of material increases the current. The ON current is improved when the gate material is Hafnium oxide.

In the core of channel, the quantization is practically 2-Dimensional. The FinFET device structure in 3-Dimens ions is designed in 3D Devedit and simulations are carried in ATLAS as shown in Fig.1. The structure is initially designed with Gate material as Air and corresponding I_DVSV_{GS} is found out. The gate material is replaced with high-*K* dielectric materials like Silicon dioxide and Hafnium oxide and the simulations are carriedout.

The front, meshing and top view of proposed FinFET is shown in Fig.2, 3, and 4 respectively. Table 1 shows the dielectric constants of gate mate-

Table 1. Dielectric constant of different materials.

Material	Dielectric constant
Air	1
SiO_2	3.9
HfO_2	22

Table 2. Parameters used in device.

Parameter	Value
Length along Z-axis	0.1 µm
Length along Y-axis	0.02 µm
Length along X-axis	0.045 µm
Gate lenth	10 nm

Table 3. Physical models used in simulation.

Model	Description
bqp	Alternative to density gradient method and gives better convergence
srh	used for minority carrier lifetimes
ni.fermi	fermi statistics effects are included to find intrinsic concentration
hcte.el	electron temperature is specified
bqp.ngamma	bqp γ factor for electrons in enabled
bqp.nalpha	bqp α factor for electrons is enabled
evsatmod	defines parallel field mobility model
fldmob	field dependent mobility is invoked

Table 4. Methods used for simulation.

Method	Description
maxtrap	specifies the repetition of trap procedure
autonr	Used to increase speed of solutions
nblockit	Used to define maximum number of block iterations
bicgst	Used in 3D simulations for bigger solutions
dvlimit	Used for potential correction

rials used in this paper. The dimensions of FinFET are given in Table.2. In order to study the device performance in all dimensions, various models and methods are used. These models and methods are shown in Table. 3, and Table. 4.

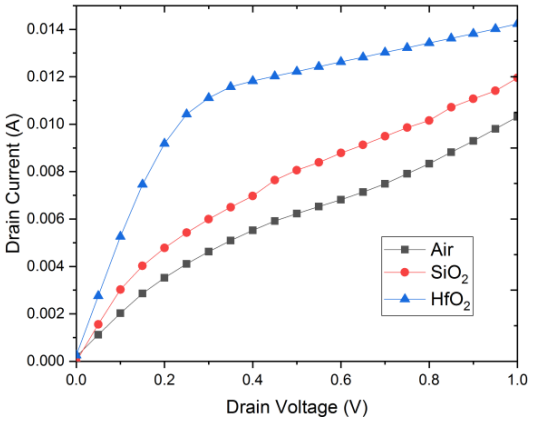

Fig. 5. I_D VS V_{DS} curves for different gate materials.

RESULTS AND DISCUSSION

Drain Current Characteristics

When the gate voltage is below threshold voltage, the device is said to be in OFF state and during this state minority charge carriers are the source for current flow. This generated current is also known as subthreshold current and is not required. The current generated when gate voltage is above threshold voltage is ON current.

The drain current vs drain voltage for dielectric materials used is shown in Fig.5. The logarithm of drain current is also shown in Fig.6.

The drain current of FinFET for Air, Silicon dioxide and Hafnium oxide materials is shown in Fig.7. The dimension of gate in all the cases is kept same. From Fig.7, we can observe that the leakage current is same in both the cases [18-20], but Hafnium oxide resulted in higher ON current than silicondioxide and Air.

With the applied gate voltage, the drain current below threshold voltage also increases. This can be viewed when the I_DVS V_{GS} graphs are plotted on logarithmic scale (as shown in Fig. 8). The drain current is increasing exponentially even below threshold voltage and it is constant after V_{GS}=0.3V. The variation in these currents is analyzed by Sub threshold slope.

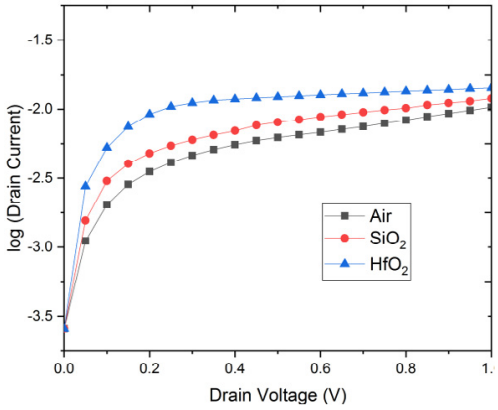

Fig. 6. log(I_D) VS V_{DS} curves for different gate materials.

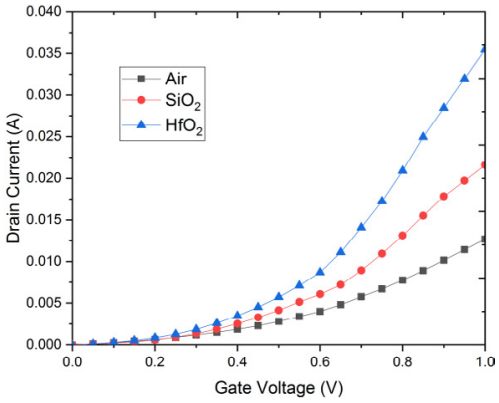

Fig. 7. I_D VS V_{GS} curves for different gate materials.

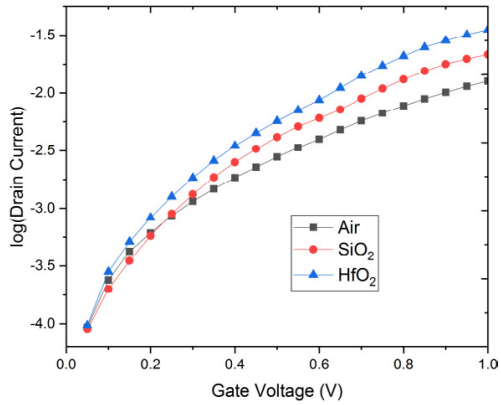

Fig. 8. log(I_D) VS V_{GS} curves for different gate materials.

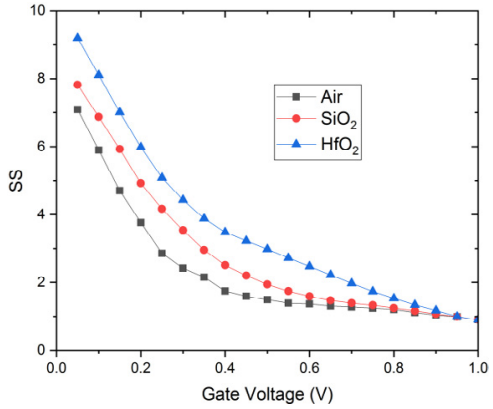

Fig. 9. Variation of SS for various gate voltages.

Subthreshold parameters

The variation even when gate voltage is below threshold voltage the current is not zero and this is specified by a parameter called Subthreshold Slope [9] given by

$$Sunthreshold\ Slope(SS) = \frac{d\,V_G}{d\left(log_{10}(I_D)\right)}$$

where V_G is applied gate voltage and I_D is resulting drain current.

Fig.9 shows the Subthreshold curve plotted for various gate voltages.The subthreshold slope is almost constant (equal to 0 mV/dec) from 0 V to 1 V is shown. To reduce the effect of heating in devices with a short channel length, a suitable value of SS is recommended.

Also the Transconductance (g_m) is plotted against various gate voltages and is shown in Fig.10. For proper gain of the amplifier high transconductance is needed [15-17].

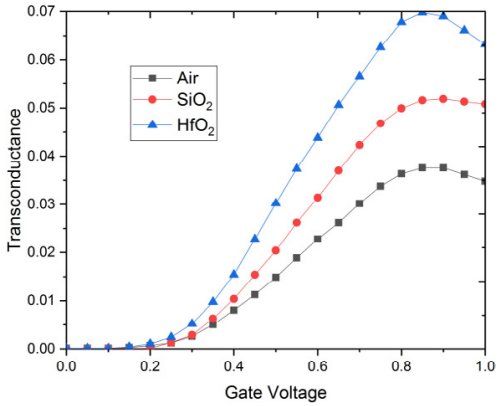

Fig. 10. Variation of g_m for various gate voltages.

$$Transconductance(g_m) = \frac{d\,I_D}{d\left(V_{DS}\right)}$$

Table.4 gives the comparison of performance

Table 5. Comparison of performance parameters.

Parameter	Air	SiO_2	HfO_2
I_{on} (A)	0.01268	0.02159	0.03546
I_{off} (A)	9.31106E-05	8.90169E-05	9.68794E-05
I_{on}/I_{off}	136.182	242.538	366.022
SS	7.09092	7.82141	9.19874
g_m	0.03757	0.05187	0.0698

parameters for different dielectric materials used.

CONCLUSION

In this paper, we have designed and simulated a new FinFET with high-*K* gate dielectric material using the concept of Effect of oxide thickness in ATLAS SILVACO and compared with similar FinFET with silicon dioxide and Air gate materials. The subthreshold slope which gives variation of drain current below threshold voltage is also calculated. The ON current is increased by a factor of ~2.79 times when the dielectric material used is HfO_2. From Table.4 there is an increase of I_{on}/I_{off}, SS and g_m by factors of 2.68, 1.3, and 1.857 respectively. Therefore, it can be concluded that the high-k gate dielectric material, Hafnium oxide FinFET has chosen the best material for proposed FinFET.

CONFLICT OF INTEREST

Authors have no conflict of interest.

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