Int. J. Nano Dimens., 13 (2): 179-196, Spring 2022

ORIGINAL ARTICLE

# Power-efficient and high-speed design of approximate full adders using CNFET technology

*Yavar Safaei Mehrabani[1,*], Mokhtar Mohammadi Ghanatghestani[2], Rabe'e SharifiRad[3], Ali Mohammad Hassanzadeh[4]*

[1] *Department of Electrical and Computer Engineering, North Tehran Branch, Islamic Azad University, Tehran, Iran*
[2] *Department of Computer Engineering, Bam Branch, Islamic Azad University, Bam, Iran*
[3] *Department of Computer Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran*
[4] *European School of Business, Reutlingen University, Reutlingen, Germany*

Received 01 September 2021; revised 28 October 2021; accepted 29 October 2021; available online 05 November 2021

**Abstract**

Full adder cells are the major fundamental elements of larger arithmetic circuits, which are mostly located along the critical path of circuits. Therefore, the design of low-power and high-speed full adder cells is critical. In this paper, there are two new inexact full adder cells proposed based on Carbon Nanotube Field Effect Transistor (CNFET) technology. Using the HSPICE simulator by applying the 32 nm Stanford model, extensive simulations are performed at the transistor level. Different supply voltages, output loads, and ambient temperatures are involved in the operation of the cells. In addition, by applying Monte Carlo transient analysis, the effects of diameter variations of carbon nanotubes (CNTs) are examined on the performance of the proposed cells. Considering the application level, these cells are studied in image processing through MATLAB software. The superiority of the proposed cells compared to their counterparts is confirmed by extensive simulations.

**Keywords:** *CNFET; Full Adder; High-Speed; Image Processing; Power-Efficient.*

**How to cite this article**

*Safaei Mehrabani Y., Mohammadi Ghanatghestani M., SharifiRad R., Hassanzadeh A.M. Power-efficient and high-speed design of approximate full adders using CNFET technology. Int. J. Nano Dimens., 2022; 13(2): 179-196.*

## INTRODUCTION

Battery-limited portable electronic gadgets are the new growing trend today. Wearable devices, smartphones, tablets, and personal digital assistants (PDAs) are some of them. Their limited battery life has made power consumption a challenge [1]. On the other hand, computing intensity is often regarded as a major characteristic of image processing algorithms [2]. Therefore, the switching speed of a circuit is regarded as another advantage. Furthermore, multimedia processing, machine learning, and data mining are among error-tolerant applications. To meliorate circuit parameters such as power consumption, latency, and area occupation, approximate computation has emerged as a plausible solution [3]. Circuits somehow can obviate hardware limitation through relaxing precision.

Applying Full Adders in adders, subtractors, multipliers, and even larger structures has made them a vital part of arithmetic circuits [4, 5]. Also, they are used in configurable logic blocks (CLBs) of field-programmable gate arrays (FPGAs) [6]. Hence, it seems necessary to design high-performance and low-power Full Adder cells. Two approximate Full Adder cells are presented in this article based on carbon nanotube field-effect transistor (CNFET) technology. They are both low-power, high-speed, and low transistor count. Standard complementary metal-oxide-semiconductor (CMOS) logic style forms the basis of the first design. However, the combination of transmission gate (TG) and pass transistor (PT)

* Corresponding Author Email: *y.safaei@iau-tnb.ac.ir*

logic is what the second design is built upon. To assess the performance of the proposed cells, they are compared with several state-of-the-art Full Adders. Considerable computer simulations are performed concerning voltage, output load, temperature, and process variations. Simulation results indicate the superiority of the proposed cells in terms of power consumption, delay, and power-delay product (PDP) figures of merit. These cells are subsequently applied in the image processing application of motion detection [7]. The peak signal-to-noise ratio (PSNR) metric is considered for examining the efficiency of approximate circuits. Consequently, the product of PDP and inverse of PSNR is considered to make a balance between the outcomes of switching and application levels.

The feature size of metal oxide semiconductor field-effect transistors (MOSFETs) has entered the nano region at 65 nm, in 2006 [8]. Silicon bulk MOSFETs encountered essential problems within the nanoscale region such as large parametric variation and an increase in leakage current [9]. To prevail over the issues of nanoscale MOSFETs, alternative post-silicon technologies have emerged. CNFET devices have the benefit of remarkable electrical characteristics [10, 11]. They inherently are high-speed and low-power due to the near ballistic conduction of charge carriers and low off-current, respectively [12]. As a result, CNFET technology is predicted to be a promising successor to traditional MOSFETs in the future. By twisting a graphite planar sheet consisting of carbon hexagons called graphene, carbon nanotubes (CNTs) are formed. They are metallic or semiconducting regarding chirality vector. The chirality vector determines the angle of the arrangement of carbon atoms along the CNT, shown by an integer pair ($n_1$, $n_2$). If $|n_1 - n_2| = 3k$ $(k \in \mathbb{Z})$ then CNT is metallic; otherwise, it is semiconducting [13]. The diameter of the nanotube is obtained through Eq. 1 [14].

$$D_{CNT}(nm) = \frac{\sqrt{3}a_0}{\pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} = 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (1)$$

Where $a_0 = 0.142\,nm$ is the interatomic distance between each carbon atom and its neighbor. Single-walled carbon nanotubes (SWCNTs) are utilized as channels of CNFET devices. CNFET devices were first developed in 1998 by Tanz *et al.* [15]. Fig. 1 shows the schematic of the CNFET device [16]. The threshold voltage ($V_{th}$) of a CNFET, as shown in Eq. 2, is inversely proportional to the diameter of carbon nanotubes [16].

$$V_{th} \approx \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} = \frac{0.43}{D_{CNT}(nm)}V \quad (2)$$

Where $a = 2.49\,\text{Å}$ is the carbon to carbon *atom* distance, $V_\pi = 3.033\,eV$ is the carbon $\pi - \pi$ bond energy in the tight bonding model, *e* is the unit charge of the electron, and $D_{CNT}$ is the diameter of the CNT. As shown in Fig. 2 there are three potential kinds of CNFETs [17, 18]. The first kind, known as Schottky-barrier (SB-CNFET), is shown in Fig. 2 (a). They are not appropriate for applications that demand high-performance operation. The

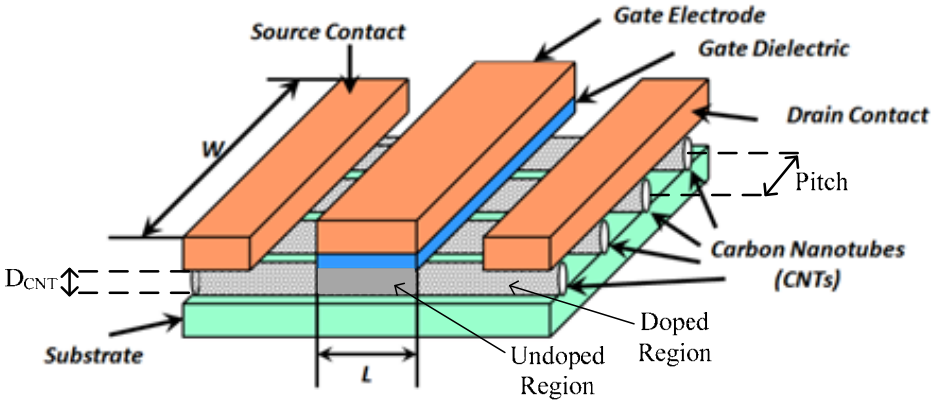



Fig. 1. Schematic of CNFET device [14].

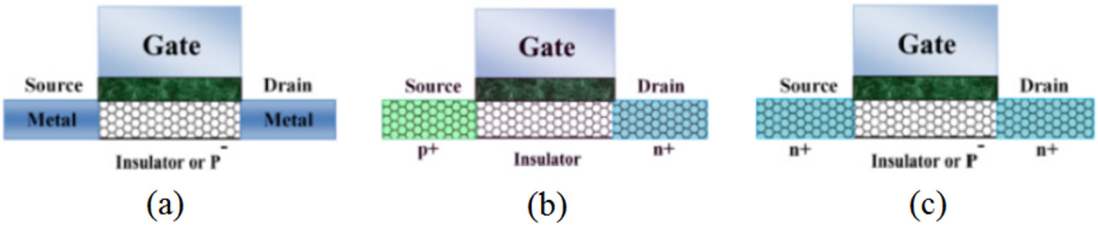



Fig. 2. Different kinds of CNFETs (a) SB-CNFET (b) T-CNFET (c) MOSFET-like [15].

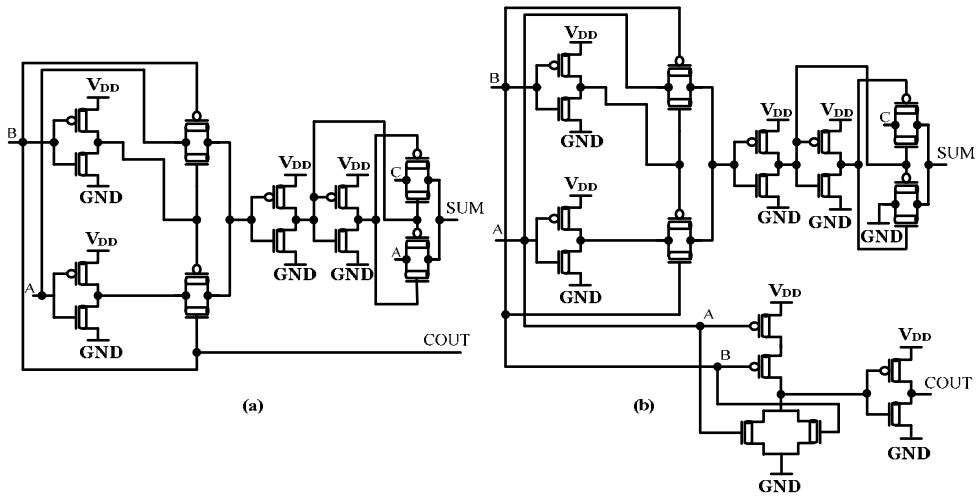



Fig. 3. The schematic of TGA designs (a) TGA1 (b) TGA2.

second kind of CNFETs is shown in Fig. 2 (b), which is known as band-to-band tunneling CNFET (T-CNFET). The low current, once the transistor is ON, makes it to be appropriate for low-power applications. The third kind, known as MOSFET-like, is doped with constant diffusion within the drain and source sides. The MOSFET-Like device is shown in Fig. 2 (c). They are appropriate for high-performance applications. From above, MOSFET-like CNFETs are used for designing the proposed Full Adder cells in this paper.

Approximate computing (AC) is an effective computational way to improve hardware criteria, i.e. power consumption, delay, and area by introducing a few errors in outputs [19]. This method is utilized in applications consisting of multimedia, machine learning, data mining, etc. About 75% of the information someone gets is through the sense of vision [20]. Accordingly, there are a big variety of digital systems designed for human interface [21]. In the following, a few key error metrics are reviewed. The first metric is known as error distance (ED). It is the mathematical distance of outputs for accurate and inexact results [22]. The error metric which is maximum ED (MAE) is used to define the maximum error distance produced through a circuit [23]. Mean error distance (MED) is the average of EDs for a given circuit. It statistically determines the efficacy of an approximate circuit in terms of accuracy [22]. Since MED depends upon the word length of the circuit, the normalized error distance (NED) is considered. The NED is acquired by dividing MED through the maximum value that is realized in a circuit [22]. Eqs. 3 and 4 calculate MED and NED metrics.

$$MED = \frac{\sum ED}{N} \tag{3}$$

$$NED = \frac{MED}{MAX} \tag{4}$$

Where *N* and *MAX* denote the number of input combinations and maximum value of output, respectively. If a circuit has lower MED or NED, it is predicted to have better accuracy.

Fig. 3(a, b) illustrates the schematic of two

transmission gate-based approximate Full Adder cells called TGA1 and TGA2 [24]. The TGA1 and TGA2 designs are consist of 16 and 22 transistors, respectively. The critical path of each design consists of 5 transistors, which is a reason for a long propagation delay. Table 1 depicts the truth table of TGA1 and TGA2 designs. Considering the truth table of the TGA1 and TGA2 designs, they introduce faulty outputs in two cases out of 8 possible combinations of inputs. The MAE, MED, and NED error parameters for TGA1 and TGA2 designs are 1, 0.25, and 0.083, respectively.

In Fig. 4 (a, b, c), the schematic of the three approximate Full Adders is shown based on the XOR gate [25]. The first design is referred to as InXA1 and consists of 8 transistors. Its critical path composes of 3 transistors. The voltage of the SUM output equals to $V_{DD}$-2$V_{th}$. Therefore, it cannot effectively drive massive loads. The second design is known as InXA2 and consists of ten transistors. The InXA2 consists of 4 transistors alongside its critical path. Both outputs of InXA2 have threshold voltage loss problems. At last, the third design is known as InXA3 and consists of 8 transistors. The InXA3 includes 4 transistors in its critical path. The InXA3 design produces a full swing signal for SUM while the Cout output has a threshold voltage drop equal to $V_{DD}$-2$V_{th}$. Also, the truth table of InXA designs is tabulated in Table 2. The MAE, MED, and NED parameters for InXA1 are 2, 0.5, and 0.166, respectively. The MAE, MED, and NED error metrics for each InXA2 and InXA3 are 1, 0.25, and 0.083, respectively.

Fig. 5 shows the schematic of the NNIFA cell [26]. It includes twelve transistors, 4 of which are located along the critical path of the Full Adder circuit. The NNIFA produces a full voltage swing signal for Cout output. Whereas, the SUM output suffers from a threshold voltage drop equal to $V_{DD}$-$V_{th}$. The truth table of the NNIFA cell is clarified in Table 3. The MAE, MED, and NED metrics for NNIFA are 1, 0.25, and 0.083, respectively.

Fig. 6 shows a transistor-level diagram of a bridge-based approximate Full Adder cell, which is known as BBIFA [27]. The BBIFA design includes twelve transistors, 4 of which are located along the critical path of the circuit. It produces full voltage swing outputs for both SUM and Cout. The truth table of the BBIFA design is tabulated in Table 4. The accuracy of the Cout signal ensures that the computational error inside the level will not be propagated to the subsequent levels. The error metrics, i.e. MAE, MED, and NED for the BBIFA cell are 1, 0.25, and 0.083, respectively.

The transistor-level design of approximate Full Adders known as 10TIFA and 6TIFA are illustrated in Fig. 7 [28]. The first design is indicated in Fig. 7 (a). It has ten transistors, 3 of them are located

Table 1. Truth table of TGA designs.

| Inputs | | | Exact Output | | TGA1 | | | TGA2 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | $C_{out}$ | Sum | $C_{out}$ | Sum | ED | $C_{out}$ | Sum | ED |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1x | 0x | 1 | 1x | 0x | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1x | 0x | 1 |
| 1 | 0 | 1 | 1 | 0 | 0x | 1x | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

Table 2. Truth table of InXA designs.

| Inputs | | | Exact Output | | InXA1 | | | InXA2 | | | InXA3 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | $C_{out}$ | Sum | $C_{out}$ | Sum | ED | $C_{out}$ | Sum | ED | $C_{out}$ | Sum | ED |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1x | 1 |
| 0 | 0 | 1 | 0 | 1 | 1x | 1 | 2 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1x | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1x | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0x | 0 | 2 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0x | 1 |

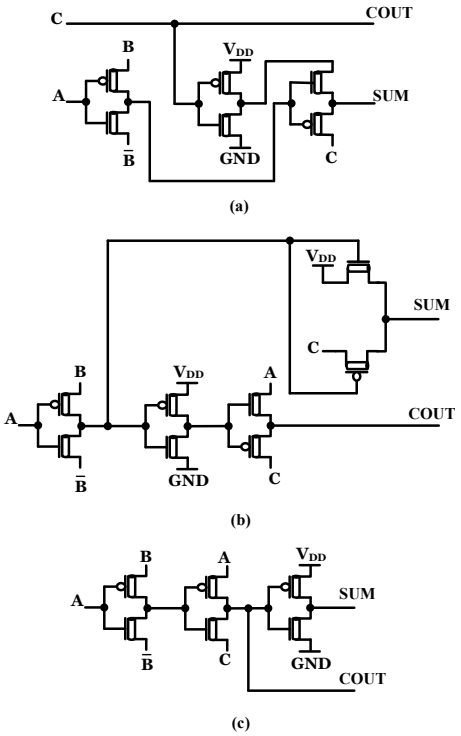



Fig. 4. The schematic of InXA designs (a) InXA1 (b) InXA2 (c) InXA3.

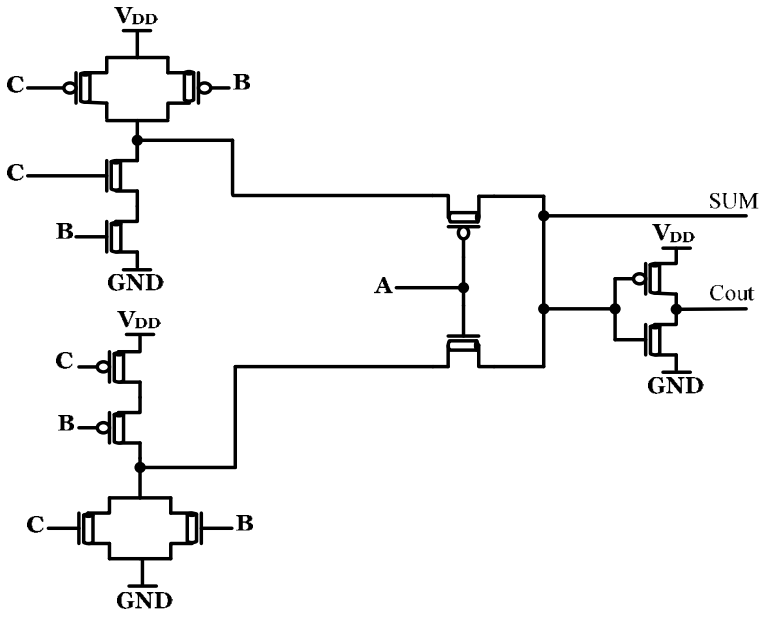



Fig. 5. The schematic of NNIFA design.

Table 3. Truth table of NNIFA design.

| Inputs | | | Exact Output | | NNIFA | | |
|---|---|---|---|---|---|---|---|
| A | B | C | $C_{out}$ | Sum | $C_{out}$ | Sum | ED |
| 0 | 0 | 0 | 0 | 0 | 0 | 1x | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0x | 1 |

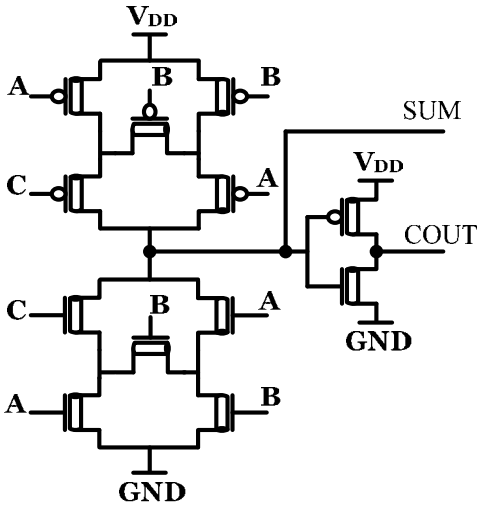



Fig. 6. The schematic of BBIFA design.

Table 4. Truth table of BBIFA design.

| Inputs | | | Exact Output | | BBIFA | | |
|---|---|---|---|---|---|---|---|
| A | B | C | $C_{out}$ | Sum | $C_{out}$ | Sum | ED |
| 0 | 0 | 0 | 0 | 0 | 0 | 1x | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0x | 1 |

along the critical path. The presence of inverter gates at the output nodes ensures the strength of the output signals. The second design is indicated in Fig. 7 (b). It has only six transistors, two of which are located along the critical path. The truth table of the 10TIFA and 6TIFA designs is tabulated in Table 5. The MAE, MED, and NED metrics for each 10TIFA and 6TIFA designs are 1, 0.375, and 0.125, respectively.

Fig. 8 shows the transistor-level design of the AFA1 structure [29]. The AFA1 consists of 8 transistors, 3 of which are located along the critical path. The truth table of the AFA1 design is shown in Table 6. It passes the error to higher significant bit positions through the Cout signal. The MAE, MED, and NED error metrics of AFA1 are 1, 0.375, and 0.125, respectively.

Finally, Table 7 tabulates all characteristics of various approximate Full Adder cells at both switching and application abstraction levels.

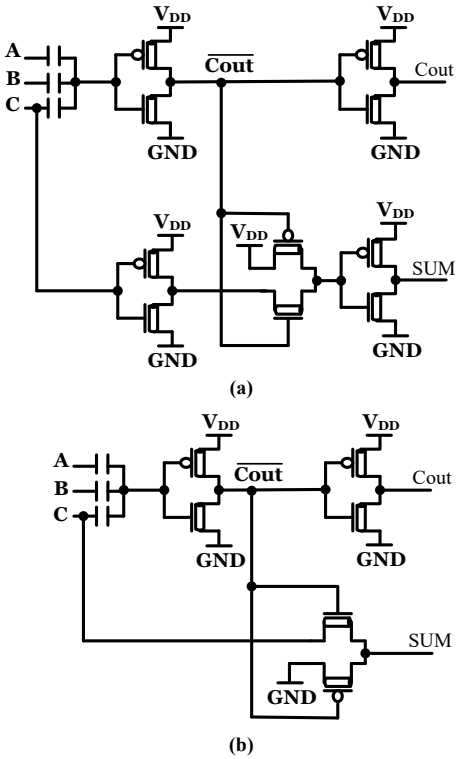



Fig. 7. The schematic of CTL based designs (a) 10TIFA (b) 6TIFA.

Table 5. Truth table of 10TIFA and 6TIFA designs.

| Inputs | | | Exact Output | | 10TIFA&6TIFA | | |
|---|---|---|---|---|---|---|---|
| A | B | C | $C_{out}$ | Sum | $C_{out}$ | Sum | ED |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0x | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0x | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0x | 1 |

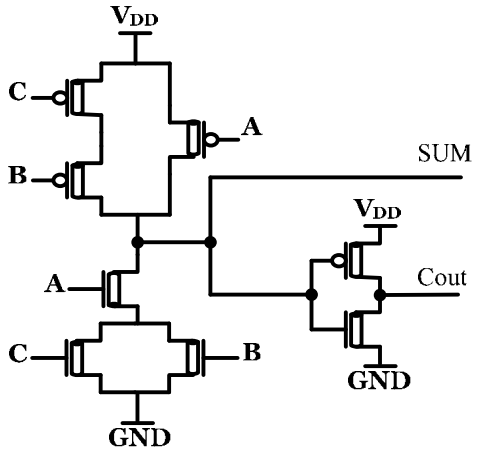



Fig. 8. The schematic of AFA1 design.

Table 6. Truth table of AFA1 design.

| Inputs | | | Exact Output | | AFA1 | | |
|---|---|---|---|---|---|---|---|
| A | B | C | $C_{out}$ | Sum | $C_{out}$ | Sum | ED |
| 0 | 0 | 0 | 0 | 0 | 0 | 1x | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0x | 1x | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0x | 1 |

Table 7. The characteristics of different designs.

| Abstraction Level | | Switching | | | | Application | | |
|---|---|---|---|---|---|---|---|---|
| Design | Ref. | #Tran. | Critical Path | Cout Swing | SUM Swing | MAE | MED | NED |
| TGA1 | [23] | 16 | 5 | YES | YES | 1 | 0.25 | 0.083 |
| TGA2 | [23] | 22 | 5 | YES | YES | 1 | 0.25 | 0.083 |
| InXA1 | [24] | 8 | 3 | YES | NO | 2 | 0.5 | 0.166 |
| InXA2 | [24] | 10 | 4 | NO | NO | 1 | 0.25 | 0.083 |
| InXA3 | [24] | 8 | 4 | NO | YES | 1 | 0.25 | 0.083 |
| NNIFA | [25] | 12 | 4 | YES | NO | 1 | 0.25 | 0.083 |
| BBIFA | [26] | 12 | 4 | YES | YES | 1 | 0.25 | 0.083 |
| 6TIFA | [27] | 6 | 2 | YES | NO | 1 | 0.375 | 0.125 |
| 10TIFA | [27] | 10 | 3 | YES | YES | 1 | 0.375 | 0.125 |
| AFA1 | [28] | 8 | 3 | YES | YES | 1 | 0.375 | 0.125 |

Table 8. Truth table of the proposed designs.

| Inputs | | | Exact Output | | Inexact Output | | |
|---|---|---|---|---|---|---|---|
| A | B | C | $C_{out}$ | Sum | $C_{out}$ | Sum | ED |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0x | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0x | 1 |
| 0 | 1 | 1 | 1 | 0 | 0x | 1x | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0x | 1 |
| 1 | 0 | 1 | 1 | 0 | 0x | 0 | 2 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

## MATERIALS AND METHODS

The proposed approximate 1-bit Full Adder designs are achieved from Table 8. In Table 8 the truth table of the mentioned designs is tabulated. The MAE parameter for the proposed truth table is 2. Also, the MED and NED parameters are 0.75 and 0.25, respectively. If we take a look at Table 8, it is inferred that the SUM and Cout outputs are realized by Eqs. 5 and 6. It is needed only 2-input AND gates to realize them. Therefore, the proposed designs will benefit from simple structures. furthermore, the switching activity (α) of the SUM and Cout signals is 0.1875 which results in low power consumption.

$$SUM = B.C \tag{5}$$

$$Cout = B.A \tag{6}$$

In Fig. 9 the structures of the proposed Full Adder cells are illustrated at the transistor level. The first design which is called 12TAFA is depicted in Fig. 9 (a). It employs the standard CMOS logic style. The second design which is called 8TAFA is shown in Fig. 9 (b). It employs the transmission gate logic style. Since all internal and external nodes of the proposed designs are full voltage swing, it results in low-power consumption and high driving ability. In other words, rail-to-rail output signals of the proposed cells ensure their proper operation in the presence of large output loads. There are three and two transistors along the critical path of the 12TAFA and 8TAFA cells,

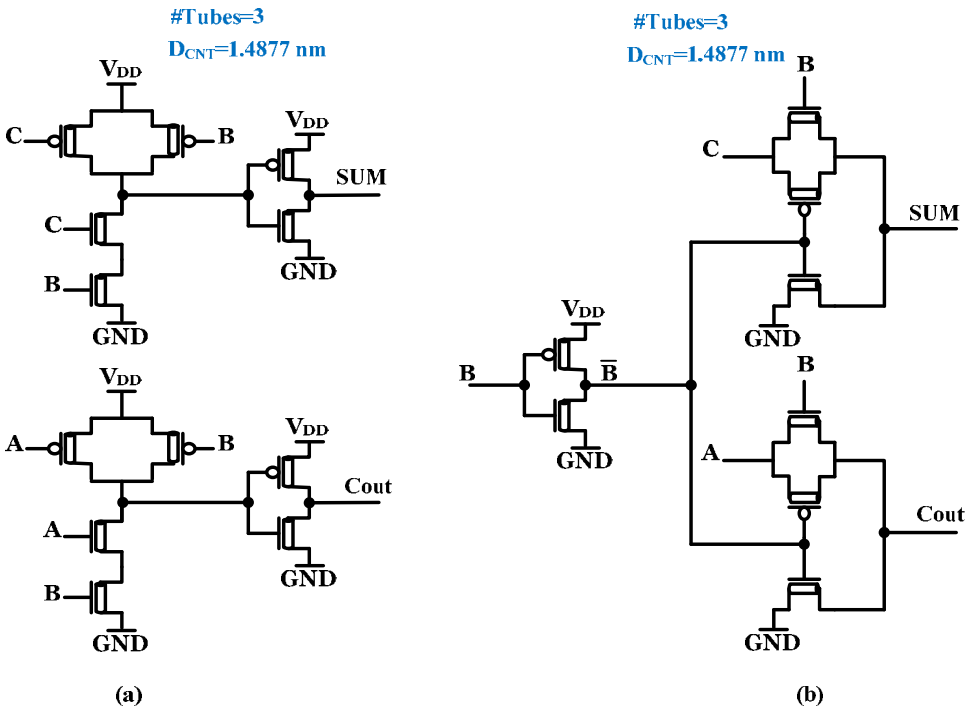



Fig. 9. The proposed Full Adders (a) 12TAFA (b) 8TAFA.

respectively. Therefore, the 8TAFA design is expected to be very high-speed. There are three tubes used in each CNFET device as a transistor channel. Besides, the diameter of all CNTs is 1.4877 nm. Fig. 10(a, b, c) depicts the transient response of the cells at 0.9V $V_{DD}$. Simulation results confirm the correct operation of the proposed designs.

## RESULTS AND DISCUSSION

*Simulation environment*

To carry out transistor-level simulations, the Synopsys HSPICE simulator is used. All designs are simulated using the 32 nm CNFET compact SPICE model [30, 31]. This model is advanced for unipolar, MOSFET-like CNFET devices. Some important parameters of this model, with brief descriptions, are tabulated in Table 9.

The simulation environment is indicated in Fig. 11. As presented in Fig. 11, realistic inputs are fed to the circuit under test (CUT) by the use of buffers. Moreover, a fanout-of-4 inverter (FO4) is used as a standard output load for SUM and Cout signals [32]. An exhaustive test pattern including all the feasible input transitions is applied to approximate Full Adders to investigate their efficiency. To get the delay of the circuit, the delay of all transitions on the output nodes is taken into account and consequently, the largest value is reported. Also, average power consumption is assessed during a long period. The power-delay product (PDP) and energy-delay product (EDP) criteria are considered [33]. Also, the power-delay-area product (PDAP) is an elegant metric to indicate the advantage of the approximate Full Adder designs.

*Switching level*

State-of-the-art approximate 1-bit Full Added cells are studied within extensive simulation conditions. They are simulated in a range of 0.8V to 1V $V_{DD}$ at the load of FO4, room temperature of 25 °C, and 1GHz operating frequency to evaluate their efficacy. The results are tabulated in Table 10. Considering Table 10, the 12TAFA and 8TAFA cells outperform their counterparts in terms of power consumption, delay, PDP, EDP, and PDAP metrics for all the supply voltages.

A broad range of loads from FO1 to FO16 at 0.9V supply voltage, room temperature, and 1GHZ operating frequency has been taken into account to simulate all circuits. Fig. 12 (a, b, c, d) illustrates the simulation results. The highest power consumption and the longest propagation delay are related to InXA3, BBIFA, InXA2, and NNIFA designs. The rising of output load will lead

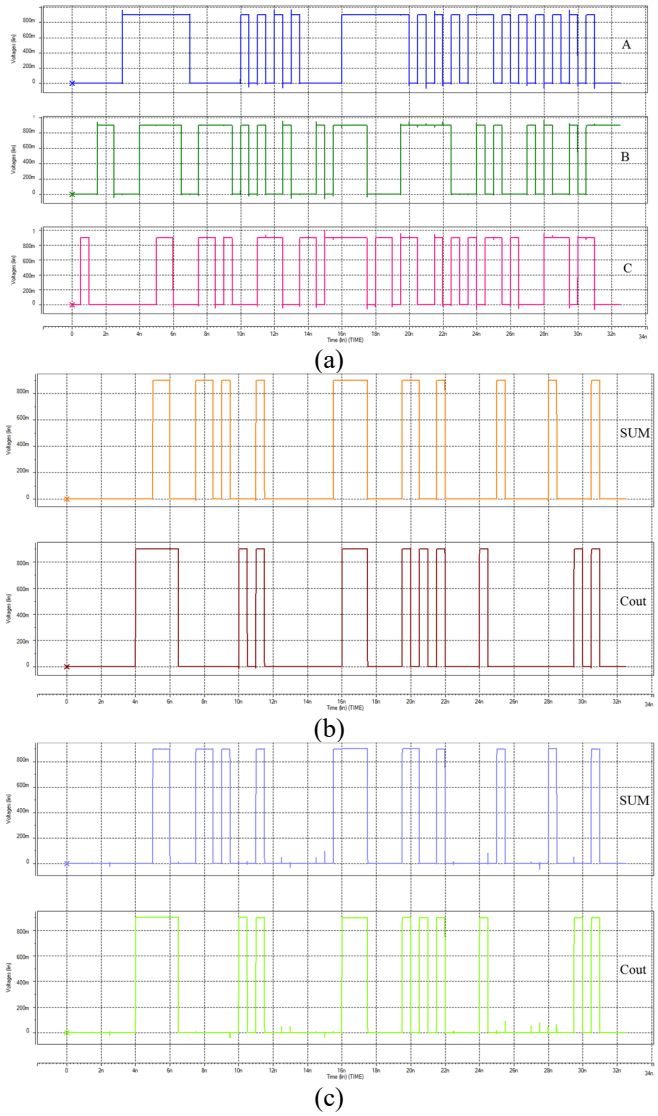



Fig. 10. Snapshot of signals (a) Inputs (b) Outputs of 12TAFA (c) Outputs of 8TAFA.

Table 9. Some input parameters of the simulation model [28, 29].

| Parameter | Value | Description |
|---|---|---|
| $L_{ch}$ | 32nm | Physical channel length |
| $L_{geff}$ | 100nm | The mean free path in the intrinsic CNT channel |
| $L_{ss}$ | 32nm | The length of doped CNT source-side extension region |
| $L_{dd}$ | 32nm | The length of doped CNT drain-side extension region |
| $K_{gate}$ | 16 | The dielectric constant of high-K top gate dielectric material |
| $T_{ox}$ | 4nm | The thickness of high-K top gate dielectric material |
| $C_{sub}$ | 40pF/m | The coupling capacitance between the channel region and the substrate |
| Efi | 0.6ev | The Fermi level of the doped S/D tube |

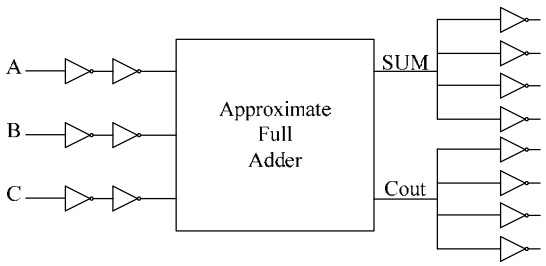



Fig. 11. Simulation testbed.

Table 10. Simulation results against different supply voltages.

| Design | Power ($10^{-6}$ W) | Delay ($10^{-12}$ S) | PDP ($10^{-17}$ J) | EDP ($10^{-29}$J.S) | Tr. No. | PDAP ($10^{-17}$ J) |
|---|---|---|---|---|---|---|
| Vdd=1V | | | | | | |
| TGA1 | 1.6602 | 13.389 | 2.2229 | 29.7624 | 16 | 35.5664 |
| TGA2 | 1.3963 | 10.749 | 1.5009 | 16.1331 | 22 | 33.0198 |
| InXA1 | 1.6645 | 10.284 | 1.7118 | 17.6041 | 8 | 13.6944 |
| InXA2 | 1.9632 | 16.846 | 3.3072 | 55.7130 | 10 | 33.072 |
| InXA3 | 1.9656 | 21.564 | 4.2387 | 91.4033 | 8 | 33.9096 |
| NNIFA | 1.6326 | 18.261 | 2.9812 | 54.4396 | 12 | 35.7744 |
| BBIFA | 1.5892 | 21.572 | 3.4283 | 73.9552 | 12 | 41.1396 |
| 6TIFA | 2.2071 | 13.485 | 2.9763 | 40.1354 | 6 | 17.8578 |
| 10TIFA | 2.1678 | 13.038 | 2.8264 | 36.8506 | 10 | 28.264 |
| AFA1 | 1.3531 | 15.943 | 2.1572 | 34.3922 | 8 | 17.2576 |
| 12TAFA [Proposed] | 1.0792 | 8.7138 | 0.94041 | 8.19454 | 12 | 11.2849 |
| 8TAFA [Proposed] | 1.0972 | 7.6710 | 0.84165 | 6.45629 | 8 | 6.7332 |
| Vdd=0.9V | | | | | | |
| TGA1 | 1.1453 | 14.226 | 1.6292 | 23.1769 | 16 | 26.0672 |
| TGA2 | 0.96517 | 11.336 | 1.0941 | 12.4027 | 22 | 24.0702 |
| InXA1 | 1.1793 | 10.593 | 1.2492 | 13.2327 | 8 | 9.9936 |
| InXA2 | 1.3242 | 18.624 | 2.4661 | 45.9286 | 10 | 24.661 |
| InXA3 | 1.3251 | 24.821 | 3.2889 | 81.6337 | 8 | 26.3112 |
| NNIFA | 1.1671 | 19.132 | 2.2329 | 42.7198 | 12 | 26.7948 |
| BBIFA | 1.1118 | 23.207 | 2.5801 | 59.8763 | 12 | 30.9612 |
| 6TIFA | 1.4460 | 16.023 | 2.3169 | 37.1236 | 6 | 13.9014 |
| 10TIFA | 1.3973 | 16.182 | 2.2610 | 36.5875 | 10 | 22.610 |
| AFA1 | 0.94111 | 16.814 | 1.5824 | 26.6064 | 8 | 12.6592 |
| 12TAFA [Proposed] | 0.74575 | 9.1198 | 0.6801 | 6.20237 | 12 | 8.1612 |
| 8TAFA [Proposed] | 0.78944 | 8.0440 | 0.6350 | 5.10794 | 8 | 5.0800 |
| Vdd=0.8V | | | | | | |
| TGA1 | 0.79941 | 15.472 | 1.2368 | 19.1357 | 16 | 19.7888 |
| TGA2 | 0.66360 | 12.496 | 0.82922 | 10.3619 | 22 | 18.2428 |
| InXA1 | 0.84766 | 11.515 | 0.97605 | 11.2392 | 8 | 7.8084 |
| InXA2 | 0.90169 | 18.301 | 1.6502 | 30.2003 | 10 | 16.502 |
| InXA3 | 0.87500 | 27.508 | 2.4069 | 66.2090 | 8 | 19.2552 |
| NNIFA | 0.76038 | 20.727 | 1.5761 | 32.6678 | 12 | 18.9132 |
| BBIFA | 0.71857 | 24.719 | 1.7762 | 43.9058 | 12 | 21.3144 |
| 6TIFA | 0.98254 | 19.678 | 1.9335 | 38.0474 | 6 | 11.601 |
| 10TIFA | 0.95222 | 19.321 | 1.8398 | 35.5467 | 10 | 18.398 |
| AFA1 | 0.57532 | 18.183 | 1.0461 | 19.0212 | 8 | 8.3688 |
| 12TAFA [Proposed] | 0.47909 | 9.5045 | 0.45535 | 4.32787 | 12 | 5.4642 |
| 8TAFA [Proposed] | 0.51611 | 8.6749 | 0.44772 | 3.88392 | 8 | 3.58176 |

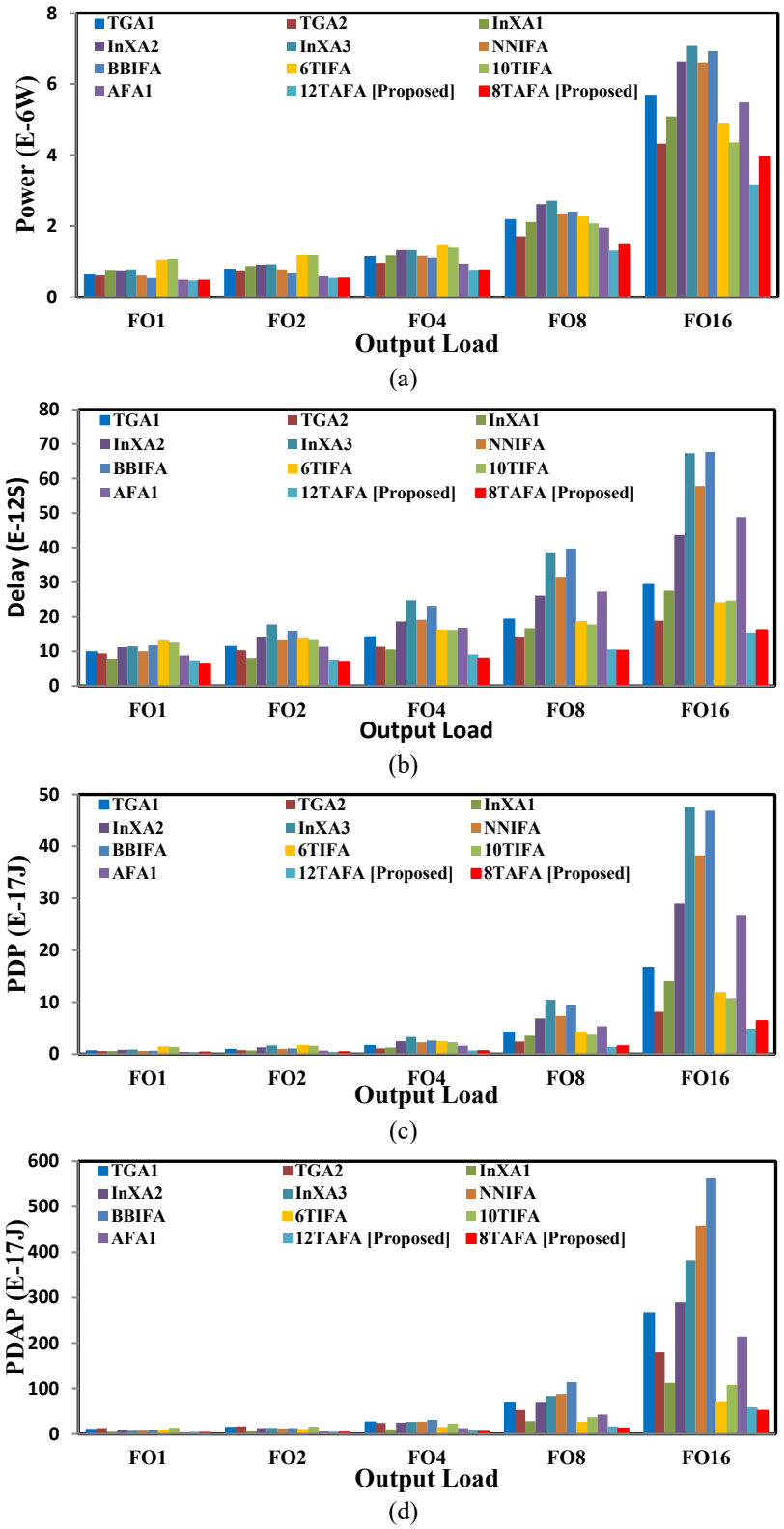
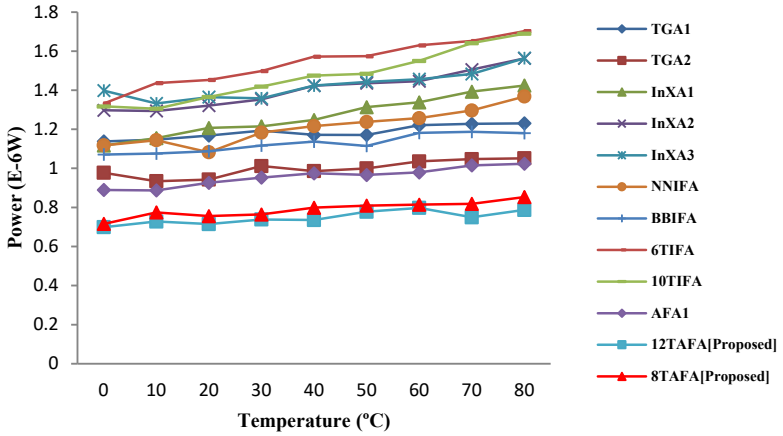


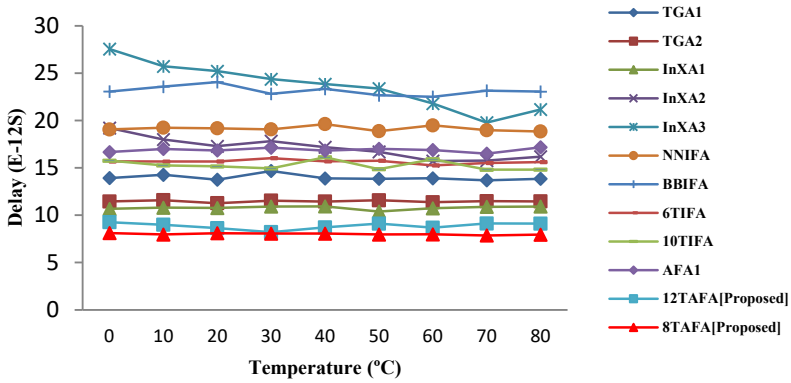

Fig. 12. Simulation results against load variations (a) Power (b) Delay (c) PDP (d) PDAP.

to a rapid increase in power consumption and delay by a faster rate compared to other circuits. The lowest power consumption, delay, PDP, and PDAP belong to the proposed 12TAFA and 8TAFA cells for all loads.

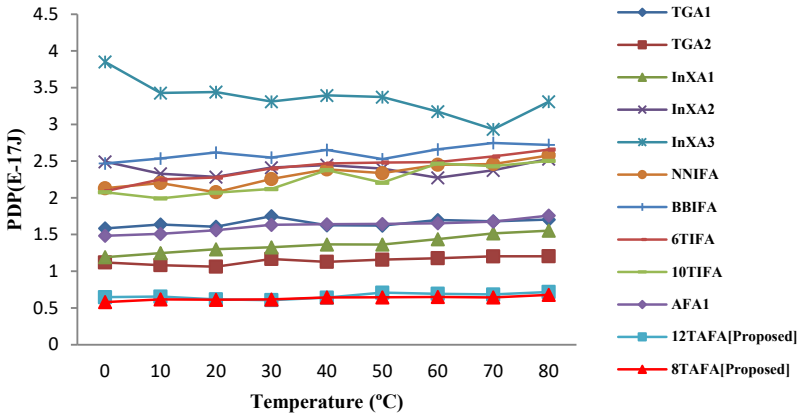
Fig. 13 (a, b, c, d) demonstrates the operation of the circuits against a wide range of temperatures from 0°C to 80°C. Considering Fig. 13, it is evident



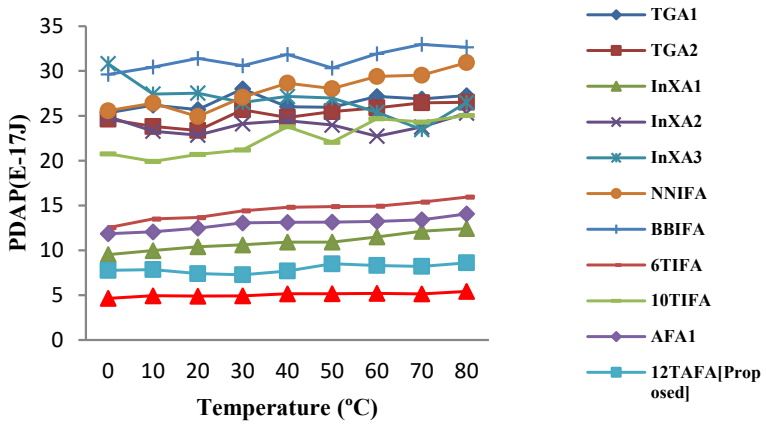

(a)




(b)




(c)




(d)

Continiued Fig. 13. Simulation results against temperature variations (a) Power (b) Delay (c) PDP (d) PDAP.

that the proposed cells function properly and are robust against temperature fluctuations. The lowest power consumption and delay are related to the proposed cells. The PDP and PDAP quantitative metrics of the proposed cells are almost fixed without any major changes.

There is a possibility that the diameter of carbon nanotubes will change [34]. Changes in diameter will shift the threshold voltage of transistors. Accordingly, there may be disruptions in the suitable operation of the circuit. Thus, a Monte Carlo (MC) transient analysis is carried out to examine the robustness of the circuits. Each simulation is performed 30 times that is reasonably and statistically significant. If a circuit properly operates for all 30 iterations, then there is a 99% probability that more than 80% of its components will work appropriately [13]. The distribution function of diameter variations of CNTs is Gaussian [35]. The range of 0.05 nm to 0.2 nm is assumed to be the range of the standard deviation (STD) from the mean CNT diameter [35]. Fig. 14 (a, b, c) demonstrates the robustness of the proposed cells against diameter mismatches of carbon nanotubes.

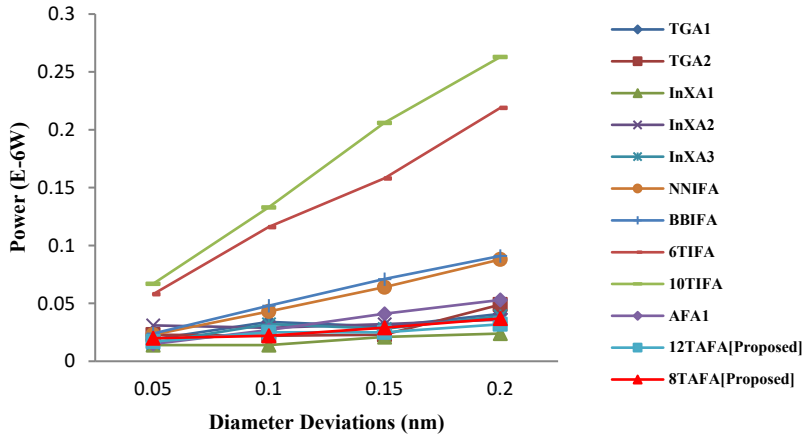
*Application level*

One of the prominent applications of image processing is the motion detection system. Pixel-by-pixel subtraction of two consecutive image frames is sufficient to detect any kind of movement. If the values of the two corresponding pixels are equal, then their difference will be zero. Therefore, it leads to the black color generation. Otherwise, shadows will appear in places where there is a movement. Subtraction operation is carried out by adding minuend to the 2's complement value of subtrahend. It is worth noting that one to four inexact Full Adder cells are utilized in the lower significant bits of the adder circuit. The simulations are performed through MATLAB software. The output images of the motion detection application are presented in Fig. 15 (a-k). An insignificant difference between accurate and inaccurate results has been observed by the output images resulting from this simulation.

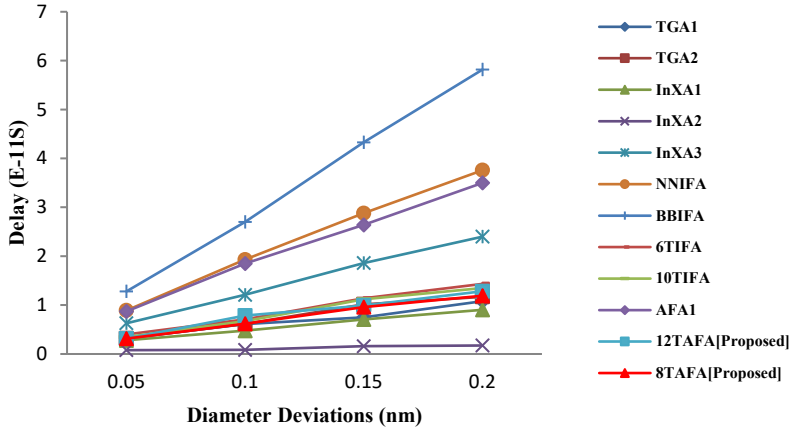
The well-recognized peak signal-to-noise ratio (PSNR) criterion is applied to assess the efficiency of circuits. Eq. 7 represents the ratio between the maximum possible power of a signal and the destructive noise power, which adversely affects the quality of the output image [36].

$$PSNR = 10\log_{10}\frac{(2^n-1)^2}{MSE} \quad (7)$$

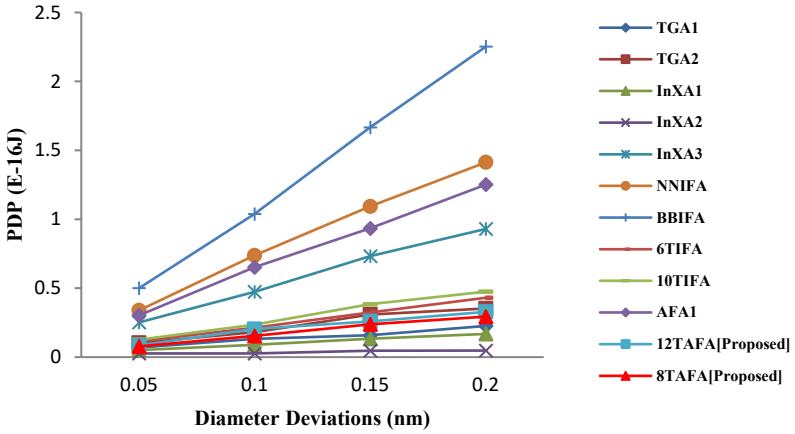
Where $n$ and $MSE$ denote the number of bits existing in each pixel and mean squared error, respectively. The $MSE$ parameter is computed using Eq. 8. In Eq. 8, $m$ and $n$ denote the numbers of rows and columns of the image. Also, $I$ and $K$ denote output images resulting from exact and inexact addition operations.




(a)




(b)




(c)

Fig. 14. Sensitivity of the circuits to the CNT diameter deviations (a) power (b) delay (c) PDP.

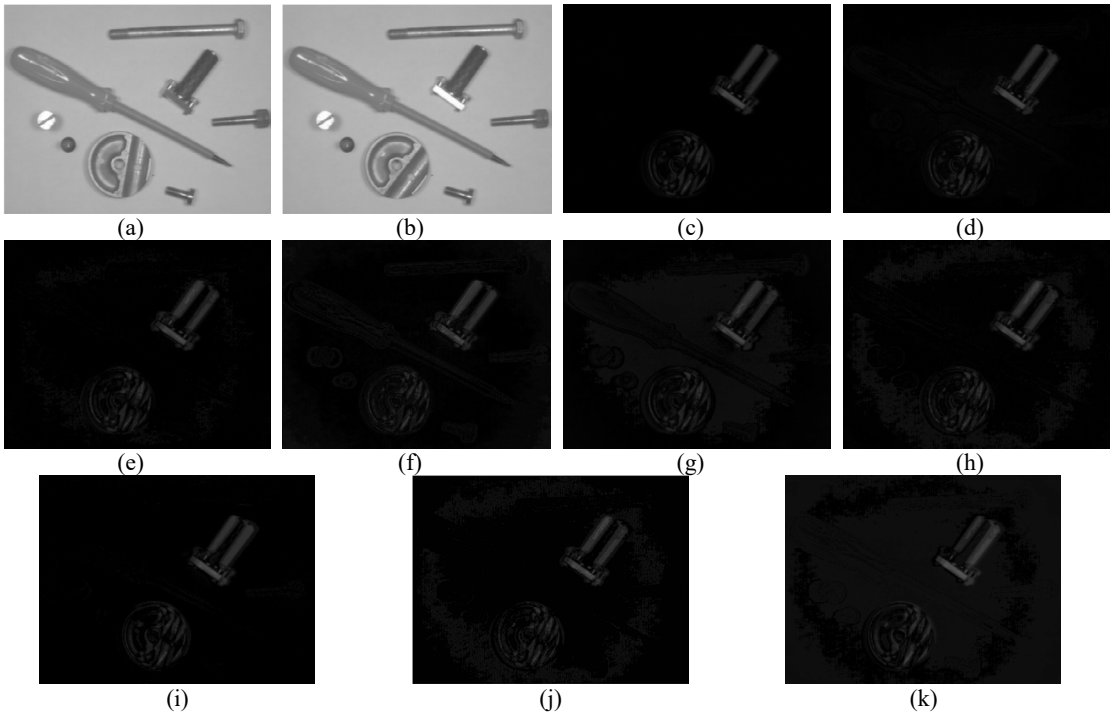



Fig. 15. Motion detection results using four inexact Full Adder cells (a) Frame 1 (b) Frame 2 (c) exact (d) TGA1 (e) TGA2 (f) InXA1 (g) InXA2 (h) InXA3, NNIFA, BBIFA (i) 6TIFA, 10TIFA (j) AFA1 (k) proposed designs.

Table 11. Figure of merit when using various numbers of inexact Full Adders.

| Inexact cells | 1 | | 2 | | 3 | | 4 | |
|---|---|---|---|---|---|---|---|---|
| Design | PSNR (dB) | FOM ($10^{-17}$J/dB) | PSNR (dB) | FOM ($10^{-17}$J/dB) | PSNR (dB) | FOM ($10^{-17}$J/dB) | PSNR (dB) | FOM ($10^{-17}$J/dB) |
| TGA1 | 55.08657 | 0.473204 | 49.45873 | 0.527049 | 43.02000 | 0.605932 | 38.59485 | 0.675406 |
| TGA2 | 55.08657 | 0.436952 | 48.34724 | 0.497860 | 42.58335 | 0.565249 | 36.55403 | 0.658482 |
| InXA1 | 49.27882 | 0.202797 | 42.40412 | 0.235675 | 36.28743 | 0.275401 | 32.25144 | 0.309865 |
| InXA2 | 53.33885 | 0.462345 | 44.18895 | 0.558080 | 37.04825 | 0.665645 | 30.15863 | 0.817709 |
| InXA3 | 53.56626 | 0.491189 | 44.95750 | 0.585246 | 38.36162 | 0.685873 | 31.93774 | 0.823827 |
| NNIFA | 53.56626 | 0.500217 | 44.95750 | 0.596002 | 38.36162 | 0.698479 | 31.93774 | 0.838969 |
| BBIFA | 53.56626 | 0.577998 | 44.95750 | 0.688677 | 38.36162 | 0.807087 | 31.93774 | 0.969423 |
| 6TIFA | 55.08657 | 0.252355 | 51.05614 | 0.272276 | 45.38365 | 0.306308 | 39.54146 | 0.351565 |
| 10TIFA | 55.08657 | 0.410444 | 51.05614 | 0.442845 | 45.38365 | 0.498197 | 39.54146 | 0.571804 |
| AFA1 | 50.44077 | 0.250971 | 44.24818 | 0.286095 | 38.33338 | 0.330239 | 31.90579 | 0.396768 |
| 12TAFA | 49.59417 | 0.164559 | 41.83603 | 0.195075 | 33.64534 | 0.242565 | 26.41190 | 0.308997 |
| 8TAFA | 49.59417 | 0.102431 | 41.83603 | 0.121426 | 33.64534 | 0.150986 | 26.41190 | 0.192337 |

$$MSE = \frac{1}{mn}\sum_{i=0}^{m-1}\sum_{j=0}^{n-1}[I(i,j)-K(i,j)]^2 \quad (8)$$

Furthermore, the product of PDAP and inverse of PSNR is taken into consideration as a desirable figure of merit (FOM). Eq. (9) calculates the mentioned FOM.

$$FOM = \frac{Power \times Delay \times Tr.\,No.}{PSNR} \quad (9)$$

As it is evident in Table 11, one to four inexact Full Adder cells are utilized in the structure of the 8-bit adder circuit. The PDAP value is obtained at 0.9V supply voltage, output load of FO4, 25°C room temperature, and 1GHz operating frequency. The proposed circuits are in close competition with their counterparts concerning the PSNR metric. From the FOM point of view which is defined in Eq. 9, the proposed designs offer the best results.

## CONCLUSION

Amongst various digital circuits, the Full Adder cell plays an important role in determining the performance of the entire digital system. As a result, in this paper, two novel low-power, high-speed, and low transistor count Full Adders were proposed by relaxation of numerical outputs. Extensive computer simulations were performed to evaluate the performance of the circuits. Their efficacy was studied within the presence of various supply voltages, output loads, and ambient temperatures by using the HSPICE simulator. Also, the robustness of the circuits against the mismatches of the diameter of the carbon nanotubes was studied by carrying out the Monte Carlo transient analysis. Moreover, the operation of the circuits was investigated at the application level using MATLAB software. Simulation results confirmed the supremacy of the proposed cells compared to their counterparts.

## CONFLICT OF INTEREST

The authors declare no conflict of interest.

## REFERENCES


[1] Safaei Mehrabani Y., Eshghi M., (2016), Noise and process variation tolerant, low-power, high-speed, and low-energy full adders in CNFET technology. *IEEE Transact. Very Large Scale Integ. (VLSI) Systems*. 24: 3268–3281.

[2] Niedzicka A., (2002), Computation-intensive image processing algorithm parallelization on multiple hardware architectures, Proceedings. *Int. Conf. Parallel Comp. Elect. Eng., Warsaw, Poland.* 446–448.

[3] Schlachter J., Camus V., Palem K. V., Enz C., (2017), Design and applications of approximate circuits by gate-level pruning. *IEEE Transact. Very Large Scale Integ. (VLSI) Systems*. 25: 1694–1702.

[4] Mohammadi Ghanatghestani M., Ghavami B., Pedram H., (2018), A ternary full adder cell based on carbon nanotube FET for high-speed arithmetic units. *J. Nanoelec. Opt. Am. Sci. Pub.* 13: 368-377.

[5] Safaei Mehrabani Y., Eshghi M., (2015), High-speed, high-frequency and low-PDP, CNFET full adder cells. *J. Circ. Sys. Computers (JCSC).* 24: 1550130-1550144.

[6] Murray K. E., (2020), Optimizing FPGA logic block architectures for arithmetic. *IEEE Transact. Very Large Scale Integ. (VLSI) Systems*. 28: 1378–1391.

[7] Rahnamaei A., Zare Fatin Gh., Eskandarian A., (2019), Design of a low power high speed 4-2 compressor using CNTFET 32 nm technology for parallel multipliers. *Int. J. Nano Dimens.* 10: 114-124.

[8] Cho G., Kim Y.-B., Lombardi F., Choi M., (2009), Performance evaluation of CNFET-based logic gates. *IEEE Instrum. Measur. Technol. Conf*. Singapore. 909–912.

[9] Sinha S. K., Kumar K., Chaudhury S., (2013), CNTFET: The emerging post-CMOS device. *Int. Conf. Signal Process. Communic. (ICSC).* Noida. 372–374.

[10] Tahaei S. H., Ghoreishi S. S., Yousefi R., Aderang H., (2019), A computational study of a carbon nanotube junctionless tunneling field-effect transistor (CNT-JLTFET) based on the charge plasma concept. *Superlatt. Microstruct.* 125: 168–176.

[11] Tahaei S. H., Ghoreishi S. S., Yousefi R., Aderang H., (2019), A computational study of a heterostructure tunneling carbon nanotube field-effect transistor. *J. Elect. Mater.* 48: 7048–7054.

[12] Sadeghi B., Vahdati R. A. R., (2012), Comparison and SEM-characterization of novel solvents of DNA/carbon nanotube. *Appl. Surf. Sci.* 258: 3086-3088.

[13] Safaei Mehrabani Y., Eshghi M., (2015), A Symmetric, multi-threshold, high-speed and efficient-energy 1-bit full adder cell design using CNFET technology. *Circ. Sys. Sig. Process.* 34: 739–759.

[14] Lin S., Kim Y. B., Lombardi F., (2011), CNTFET-based design of ternary logic gates and arithmetic circuits. *IEEE Trans. Nanotechnol.* 10: 217–225.

[15] Tans S. J., Verschueren A. R. M., Dekker C., (1998), Room-temperature transistor based on a single carbon nanotube. *Nature.* 393: 49–52.

[16] Shahi A. A. M., Zarkesh-Ha P., Elahi M., (2012), Comparison of variations in MOSFET versus CNFET in gigascale integrated systems. *IEEE 13th Int. Symp. Quality Elect. Des.* 378–383.

[17] Mohammadi Ghanatghestani M., Pedram H., Ghavami B., (2015), Design of a low-standby power and high-speed ternary memory cell based on carbon nanotube FET. *J. Comput. Theoret. Nanosci. Am. Sci. Pub.* 12: 5457-5462.

[18] O'Connor I., Liu J., Gaffiot F., Prégaldiny F., Lallement C., Maneux C., Goguet J., (2007), CNTFET modeling and reconfigurable logic-circuit design. *IEEE Transact. Circ. Sys. I: Reg. Papers.* 54: 2365–2379.

[19] Xu Q., Mytkowicz T., Kim N. S., (2015), Approximate computing: A survey. *IEEE Design & Test.* 33: 8–22.

[20] Jothin R., Mohamed M. P., Vasanthanayaki C., (2020), High performance compact energy efficient error tolerant adders and multipliers for 16-bit image processing applications. *Microproc. Microsys.* 78: 103237-103241.

[21] Rostami D., Eshghi M., Safaei Mehrabani Y., (2021), Low-power and high-speed approximate 4 : 2 compressors for image multiplication applications in CNFETs. *Int. J. Elec.* 108: 1288-1308.

[22] Liang J., Han J., Lombardi F., (2012), New metrics for the reliability of approximate and probabilistic adders. *IEEE Transact. Comput.* 62: 1760–1771.

[23] Liu W., Zhang T., McLarnon E., O'Neill M., Montuschi P., Lombardi F., (2019), Design and analysis of majority logic based approximate adders and multipliers. *IEEE Transact. Emerg. Top. Computing (TETC).*10: 83-87.

[24] Yang Z., Han J., Lombardi F., (2015), Transmission gate-based approximate adders for inexact computing. *IEEE/ ACM Int. Symp. Nanosc. Archit. (NANOARCH´15), Boston.* 145–150.

[25] Almurib H. A. F., Kumar T. N., Lombardi F., (2016), Inexact designs for approximate low power addition by cell replacement. *IEEE Design, Automat. Test Europe Conf. Exhib. (DATE), Dresden.* 660–665.

[26] Safaei Mehrabani Y., Faghih Mirzaee R., Zareei Z., Daryabari S. M., (2017), A novel high-speed, low-power CNTFET-based inexact full adder cell for image processing application of motion detector. *J. Circ. Sys. Comput. (JCSC).* 26: 1750082-1–1750082-15.

[27] Goyal C., Ubhi J. S., Raj B., (2019), A low leakage TG-CNTFET–based inexact full adder for low power image processing applications. *Int. J. Circ. Theory and Applicat.* 47: 1446–1458.
[28] Ataie R., Emrani Zarandi A. A., Mehrabani Safaei Y., (2019), An efficient inexact full adder cell design in CNFET technology with high-PSNR for image processing. *Int. J. Elect.* 106: 928–944.
[29] Mirzaei M., Mohammadi S., (2020), Process variation-aware approximate full adders for imprecision-tolerant applications. *Comput. Elect. Eng.* 87: 106761-106765.
[30] Deng J., Philip Wong H-S., (2007), A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region. *IEEE Transact. Elec. Dev.* 54: 3186–3194.
[31] Deng J., Philip Wong H-S., (2007), A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part II: Full device model and circuit performance benchmarking. *IEEE Transact. Elect. Dev.* 54: 3195–3205.
[32] Harris D., Sutherland I., (2003), Logical effort of carry propagate adders. The thrity-seventh asilomar conference on signals, systems & computers, 2003, *Pacific Grove, CA, USA.* 873–878.
[33] Govindarajulu S., Prasad T. J., (2008), Considerations of performance factors in CMOS designs. *Int. Conf. Elect. Des.,* Penang. 1–6.
[34] Cho G., Kim Y., Lombardi F., (2009), Assessment of CNTFET based circuit performance and robustness to PVT variations. *52 nd IEEE Int. Midwest Symp. Circ. Sys.* Cancun. 1106–1109.
[35] El Shabrawy K., Maharatna K., Bagnall D., Al-Hashimi B. M., (2010), Modeling SWCNT bandgap and effective mass variation using a monte carlo approach. *IEEE Transact. Nanotechnol.* 9: 184–193.
[36] Dosselmann R., Dong Yang X., (2005), Existing and emerging image quality metrics. *Canad. Conf. Elect. Comput. Eng.* Saskatoon, Sask. 1906-1913.