

## Low-power min/max architecture in 32 nm CNTFET technology for fuzzy applications based on a novel comparator

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### Abstract

In this paper, the design of a novel low-power Min/Max circuit using Carbon Nanotube Field-Effect Transistor (CNTFET) technology has been discussed. By employing a new structure for the implementation of digital comparator, a high performance configuration has been obtained which consumes small area on chip due to the low transistor count used for its implementation. Because the comparator is capable of comparing 4-bit words, the designed circuitry can also be expanded to operate as a Winner-Takes-All (WTA) or Loser-Takes-All (LTA) system. The circuit is first simulated in a Complementary Metal-Oxide-Semiconductor (CMOS) process to demonstrate its correct performance and then, the simulations have been performed for the CNTFET technology to indicate that the design procedure is independent of the employed technology. In order to show the advantages of the proposed circuitry in a better manner, the state-of-the-art similar works have been redesignated and simulated along with our work. Based on the simulation results for CNTFET 32 nm standard process, the proposed comparator consumes  $8.3\mu\text{W}$  from 0.9V power supply, while its total transistor count is 66.

**Keywords:** CNTFET; Comparator; Fuzzy Systems; Low Power; Min/Max Circuits.

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### INTRODUCTION

Because of the analogue nature of our environment, we are always seeking for the methods and algorithms to implement and model the incidents around us in system-level as well as the hardware level. The literature review suggests that in most cases where the emphasis is on the environmental event, a fuzzy approach is one of the choices of interest for solving special purpose real problems [1]. There are numerous applications in the industry pertaining to this criterion which are dealing with the analogue signals [2]. On the other hand, there are several cases pertaining to the modeling of the biological incidents in which utilization of the neural networks seems to be the best choice [3].

As a consequence, the two common approaches which are widely used to deal with the analogue signals include fuzzy systems and neural networks.

The concept of neural computing is elder than its fuzzy counterpart due to the reports of McCulloch and Pitts in 1943 for the development of first computing neuron [4]. However, there has always been a narrow competition among these procedures due the technology improvements and it's the application that determines which approach is dominant.

There are many reports of hardware implementation for fuzzy systems as well as neural networks to confirm the efficiency of both methods. In addition, both approaches can be realized by means of digital, analogue or mixed-mode circuit design techniques [5-6]. For a fuzzy system, the basic building blocks include fuzzifier, inference engine, and defuzzifier, where the Min/Max circuits constitute the main sub-block for the implementation of these sections (especially the inference engine).

By considering the Min/Max operation as one

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of the fundamental operands on the implementation of a fuzzy logic system due to its resemblance to AND/OR gates for logic operations [7], too many attempts have been performed for hardware level realization of Min/Max architectures [8-14] which have their own concept along with their advantages and drawbacks. In [8] and [11], achieving high precision was the main focus, while in [9] and [10] the addition of number of inputs was the main emphasis. The authors in [13] have considered the speed improvement while the architecture of [14] was based on the power reduction of whole structure.

As a summary, one of the most functional approaches for the circuit level implementation of Min/Max operation is the employment of comparator based architectures [13, 15] which is illustrated in Fig. 1. The reason somehow pertains to the decision making nature of such circuits where the accuracy of decision can be enhanced by improvement of the resolution in the comparator circuitry. This task has been successfully carried out in the previous work by the authors reported in [13] in which a resolution of 9-bit has been achieved for the comparator.

By following the comparator based idea, a novel circuit is presented in this paper which can distinguish the maximum and minimum values between two 4-bit numbers. However, a point that must be taken into account is the rapid developments of the submicron technologies on the design and implementation of Integrated Circuits (ICs). One of those enhancements belongs to the

Carbon Nanotubes (CNTs) where the scales of nanometer determine their diameter size [16]. Such feature opens the doors of better opportunities for the researchers on the power and area reduction of electronic schemes. An investigation through the literature reveals that Single-Wall CNTs (SWCNTs) have shown better properties compared to the other classes for the fabrication of ICs [17] although CNT Field-Effect Transistor (CNTFET) needs more attention from the circuit designers to fulfill the market demands in the different aspects of industry [18].

However and during the recent years, there have been many attempts for the circuit-level implementation of CNTFET schemes where several works were reported in this criterion [19, 20]. A same story goes on for the hardware implementation of neural networks [21] where a thorough analysis demonstrates that all of the published schemes in this group can be divided into two categories: modeling and fabrication. For the former class, the modeling has been done by means of Artificial Neural Networks (ANNs) [22-24], while in the latter case; the concentration was set on the fabrication [25-27]. We can also observe a similar story for the circuit-level realization of fuzzy systems and plenty of works can be found in the literature especially for the design of Min/Max circuits [28-30].

The main emphasis in this work was set on the reduction of power and active area (on chip) for the Min/Max circuit with the help of employing new structure on the design of digital comparator.

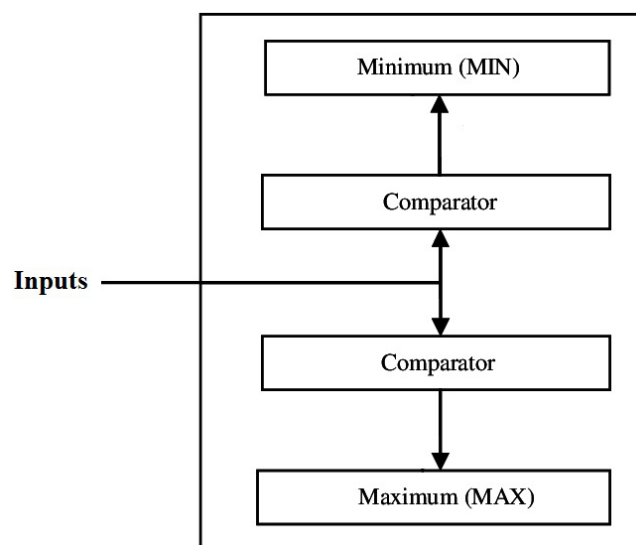


Fig. 1. General concept of the comparator based min/max.

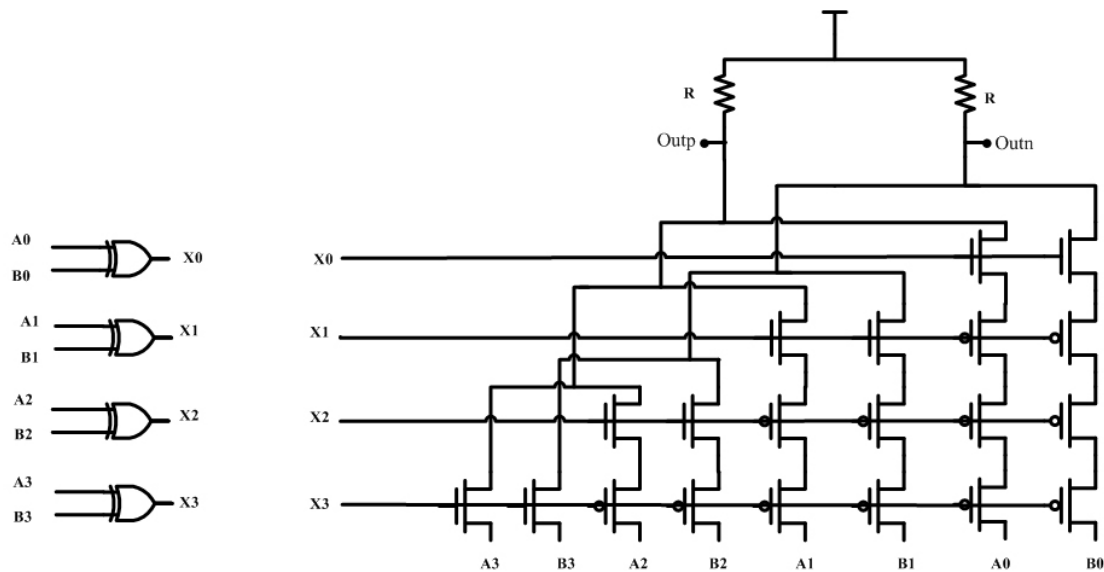


Fig. 2. Proposed 4-bit digital comparator.

By using such concept, a low power architecture consisting of 66 transistors has been proposed which can successfully detect the maximum and minimum value between two input words which is somehow based on the binary search algorithm.

The paper has been organized as follows. In section 2, the design of digital multiplier along with the proposed Min/Max structure will be discussed. Section 3 pertains to the simulation results along with the comparisons and finally, the conclusions will be provided in section 4.

**EXPERIMENTAL**

*A. Digital Comparator*

Since the emphasis in this work is on the design of 4-bit digital comparator, an investigation through the literature reveals that there can be found many works for the realization of such comparator [31-34]. While the concentration in [32] was on the system-level implementation of digital comparator, gate-level design has been focused in [31] and [33]. The architecture discussed in [34] was based on the transistor level implementation of the comparator.

Following the primary concept for the design of digital comparator, the main emphasis in this paper is on the circuit level implementation where power decrement along with the reduction of active area consumption (on chip) will constitute the other important objectives.

The proposed 4-bit comparator is shown in Fig. 2. The operating principle of this structure is almost based on the binary algorithm. At the first step,  $A_3$  and  $B_3$  bits of the inputs which constitute the Most Significant Bits (MSBs) are being compared and if the corresponding values of these bits won't be equal, then the result of decision will be clarified at this step. For  $A_3 = 1$ , and  $B_3 = 0$ , it is clear that number  $A$  defined as  $A_3A_2A_1A_0$  will be greater than number  $B$  (which is defined as  $B_3B_2B_1B_0$ ). As a result, the NMOS transistors with connected gates to  $X_3$  will be ON and the values of  $A_3$  and  $B_3$  bits will be transmitted to  $Outp$  and  $Outn$  nodes, respectively via these transistors. The same process will be repeated for  $A_3 = 0$ , and  $B_3 = 1$ . But if the logic values of  $A_3$  and  $B_3$  are equal to each other, then the output  $X_3$  will be equal to logic zero value, making the PMOS transistors (where their gates are connected to  $X_3$ ) become ON. Hence, the comparison process will be transferred to  $A_2$  and  $B_2$  bits.

This process will continue until the decision process is finished. If both of the inputs are identical, then both of  $Outp$  and  $Outn$  nodes will be charged to the high-level voltage. Therefore, the resistors can be substituted with current sources having low currents. It is worth to mention that for standard CMOS technologies the passing current through the transistors abides by the following expression [35]:



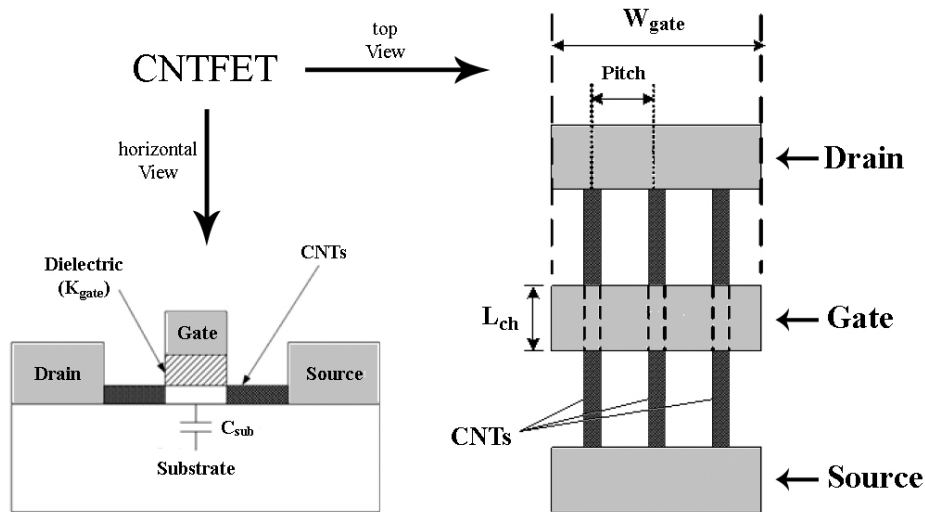


Fig. 3. Structural view of a CNTFET.

$$I_{ds} = \frac{1}{2} \mu c_{ox} \left( \frac{W}{L} \right) (V_{gs} - V_{th})^2 \quad (1)$$

where  $W$ ,  $L$ ,  $V_{gs}$  and  $V_{th}$  represent width, length, gate-source voltage and threshold voltage, respectively. Moreover,  $c_{ox}$  denotes the oxide capacitance and  $\mu$  defines the mobility parameter. But for CNTFET technologies, the story somehow differs. Depending on the region of operation along with the type of the employed CNTFET, (1) will alter and the corresponding drain current has to be calculated [36]. For instance, thorough analysis has been presented in [37] to obtain the drain current when  $SiO_2$ ,  $ZrO_2$ , and  $HfO_2$  are used for the oxide of the channel.

For a better realization of the differences between two technologies, the scheme of Fig. 3 has been demonstrated where two separate views are used to illustrate a CNT based Field Effect Transistor (FET). Based on the shown scheme, the CNT channel region is undoped, while the other regions are heavily doped making them act as the source/drain extended region. As a consequence, the gate oxide has little effect in CNTFET technologies.

However, as the emphasis in this work is on the structural-level design of the comparator, we don't deal with such equations or discussions, because the general concept of comparator design is the same for different technologies.

### B. Proposed Min/Max Architecture

With the help of the Multiplexers (MUXs)

shown in Fig. 4 and by applying the bits of input words one by one as the inputs of MUX gates along with  $Outp$  and  $Outn$  outputs in Fig. 2 (as the control signals of MUXs), the architecture of proposed Min/Max circuit will be obtained which is shown in Fig. 5.

As explained in the previous section, for the case of equal input bits, the Min and Max value will be identical which means that the MUX gates will transmit both values as Min and Max results to the output nodes.

If  $A > B$ , then the  $Outp$  control signal will transmit the maximum value to the output node, while  $Outn$  has the responsibility of choosing the minimum value between the input signals. On the other hand, for the case of  $A < B$ , the  $Outn$  control signal will transmit the maximum value to the output node.

## RESULTS AND DISCUSSIONS

To evaluate the correct behavior of the proposed Min/Max architecture and also, to demonstrate that the design procedure is independent of the employed technology, simulations are performed for both CMOS and CNTFET technologies. The proposed scheme is simulated using TSMC 0.18  $\mu m$  CMOS standard process (with 1.8 V power supply) by HSPICE for indication of the correct performance. The result which is shown in Fig. 6 for the max operation depicts that the designed architecture performs its task perfectly. It is worth to mention that in the proposed architecture of

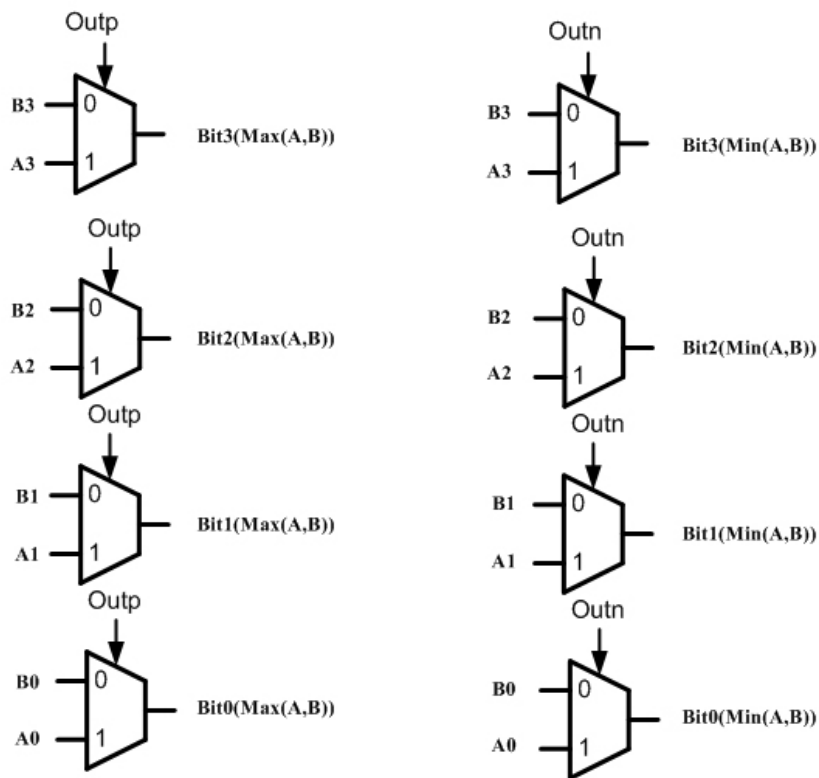


Fig. 4. MUX configuration for Min/Max design.

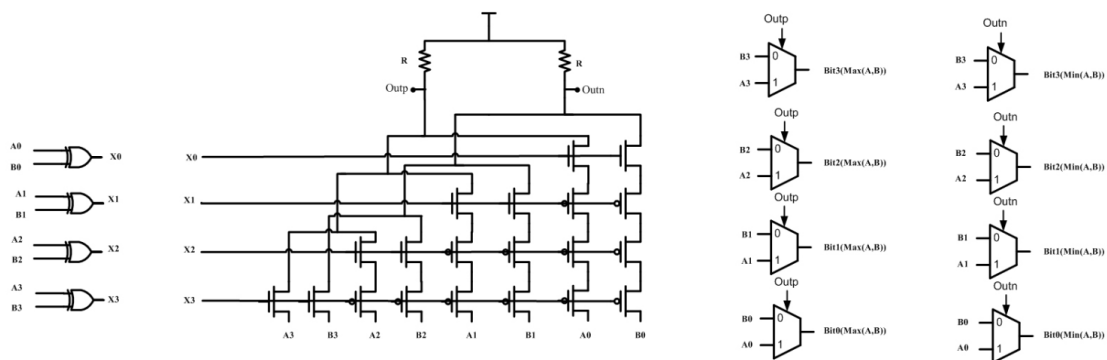


Fig. 5. Proposed Min/Max architecture.

Fig. 2, the complement transistors have been employed for the correct operation of the comparator scheme. As a consequence, the total transistor count will be 66, while the investigation of Fig. 2 demonstrates that only 46 transistors are utilized.

At the second step, the designed architecture is simulated in CNTFET 32 nm standard process by means of 0.9V power supply where the results are illustrated in Fig. 7. In Fig. 7 (a), the max output and in Fig. 7 (b), the min operation results are

shown, respectively. Based on the presented results, the correctness of the design considerations is justified again.

In order to show the variations of power dissipation with respect to the changes in supply voltage, the supply voltage has been swept and the variations were measured by means of the simulation results for both CMOS and CNTFET technologies. As Fig. 8 illustrates, the utilization of CNTFET process results in an ultra low-power system,

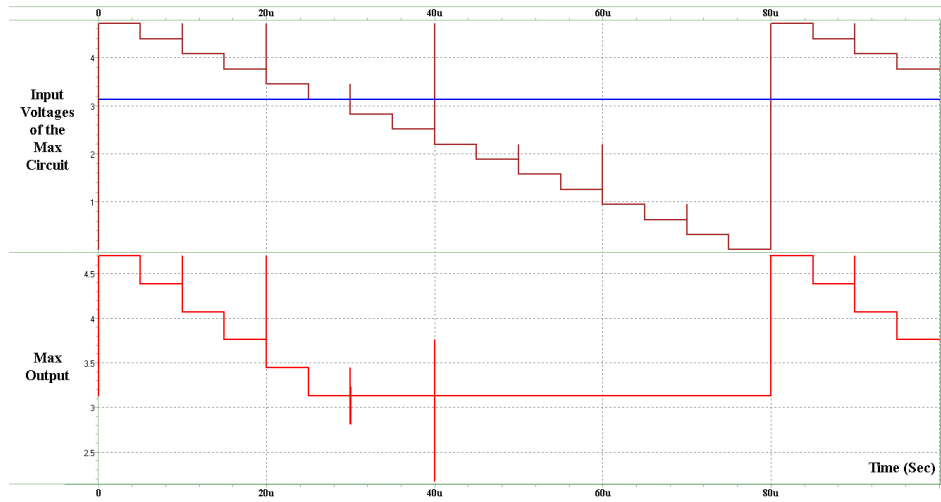
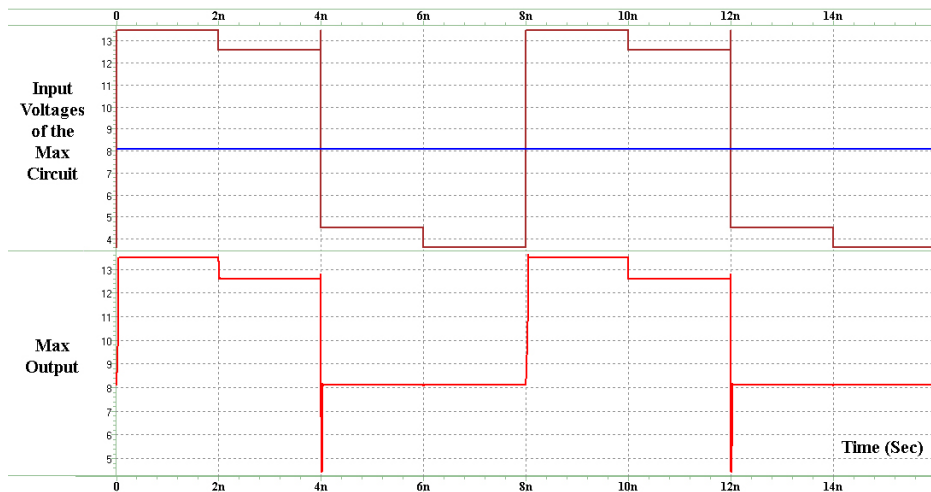
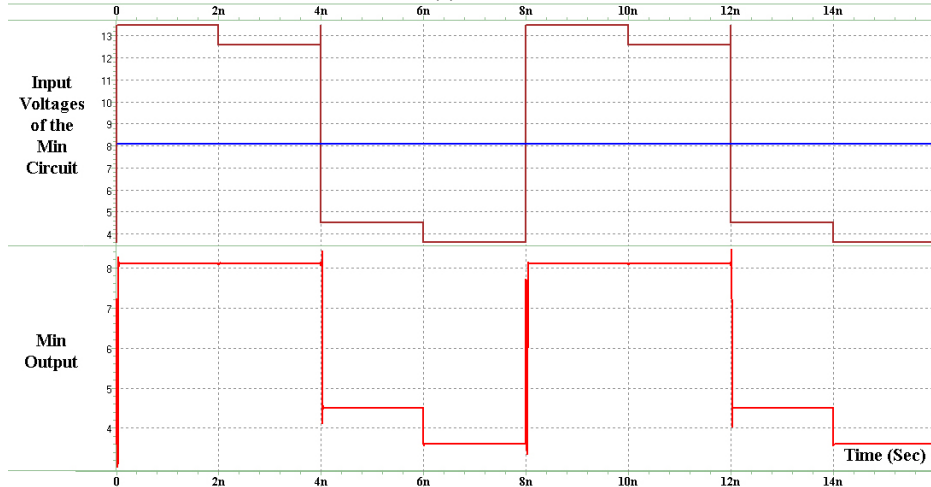


Fig. 6. Simulation results for the Max operation in 0.18 $\mu$ m CMOS process.



(a)



(b)

Fig. 7. Simulation results in CNTFET 32 nm process (a) for the Max operation (b) for the Min operation.

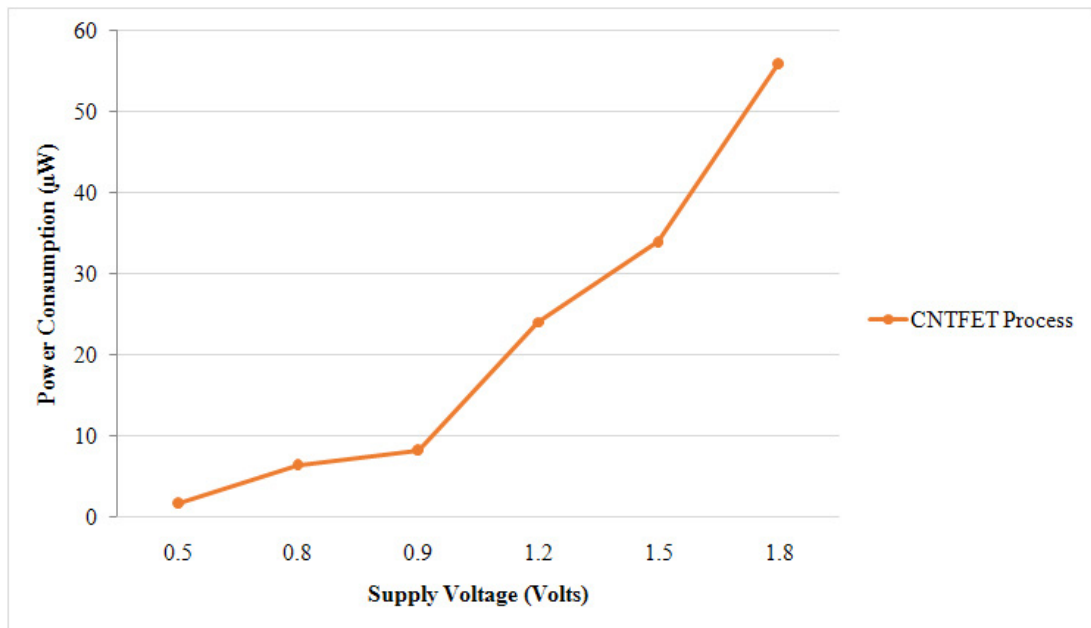


Fig. 8. Variations of power dissipation with respect to the changes in the supply voltage for CNTFET process.

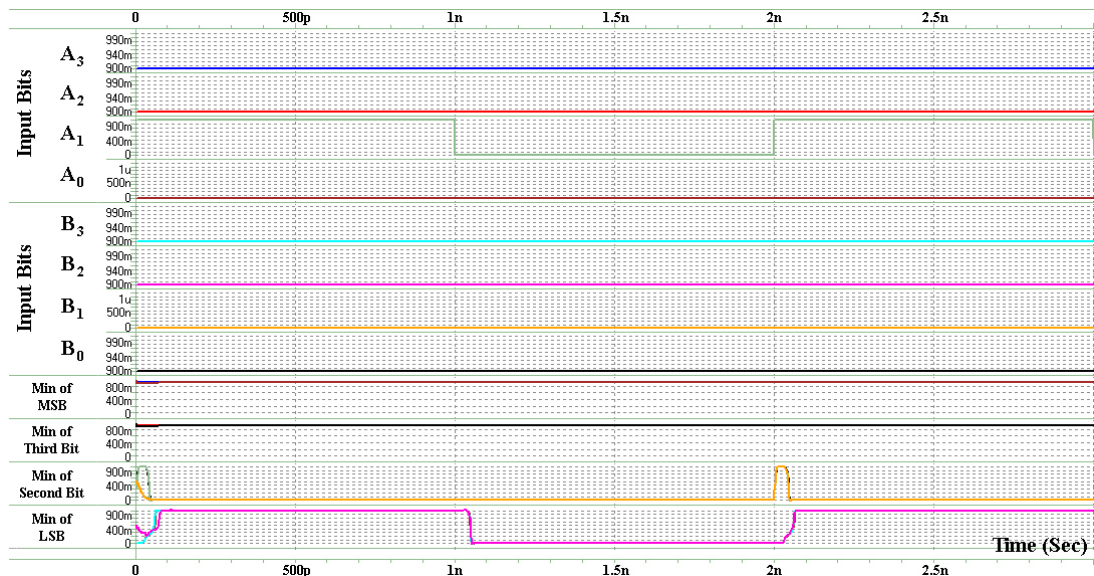


Fig. 9. The effect of temperature variations on the performance of the proposed scheme for the Min output.

because the power consumption of the proposed scheme for the 1.8 V power supply of TSMC technology was 156  $\mu$ W (based on the simulation results).

Therefore, the proposed scheme can widely be employed in low power Min/Max circuit design. Also, because of structural simplicity, the idea can

be extended for the implementation of Winner-Takes-All (WTA) and Loser-Takes-All (LTA) architectures, too.

Finally, the performance of designed Min/Max circuit is investigated by considering the effect of temperature variations. As a consequence, the temperature was swept from  $-20^{\circ}\text{C}$  to  $40^{\circ}\text{C}$  in

TABLE 1. COMPARISON BETWEEN THE PROPOSED COMPARATOR AND PREVIOUS ARCHITECTURES REPORTED IN [34].

4-Bit Comparator	CMOS [34]	TG [34]	PTL [34]	Proposed
V <sub>dd</sub>	0.9	0.9	0.9	0.9
Transistor Count	176	116	56	66
Power ( $\mu$ W)	84.2	54.2	27.4	8.3
Technology (nm)	32	32	32	32
Process	CNTFET	CNTFET	CNTFET	CNTFET

(TG = Transmission Gate , PTL = Pass-Transistor Logic)

the CNTFET technology in the HSPICE simulation environment. The result has been demonstrated in Fig. 9 for the min operation, which indicates that the proposed scheme operates correctly even for the changes of temperature at a wide range.

To show the superiority of the proposed comparator over the previous designs, the implemented architectures in [34] were redesignated and simulated by HSPICE using CNTFET 32nm standard process and 0.9V power supply voltage. Based on the results which are summarized in Table 1, the designed 4-bit comparator outperforms previous works from the viewpoint of power consumption.

## CONCLUSIONS

With the help of a novel low-power 4-bit comparator, high-performance Min/Max circuit has been proposed which can widely be employed in fuzzy logic systems for the rule selection. By employing a new structure for the implementation of digital comparator, a flexible configuration has been obtained which consumes small area on chip due to the low transistor count used for its implementation. Because the comparator is capable of comparing 4-bit words, the designed circuitry can also be expanded to operate as a WTA or LTA system.

Comparison with the similar works demonstrates the superiority of the proposed circuitry when all of the previously published schemes have been redesignated and simulated along with our circuit. Based on the simulation results for CNTFET 32 nm standard process, power dissipation of the proposed comparator circuit is 8.3  $\mu$ W from 0.9 V power supply while the total transistor count is 66.

## CONFLICT OF INTEREST

The authors declare no conflict of interest.

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