Int. J. Nano Dimens., 14 (1): 91-102, Winter 2023

ORIGINAL ARTICLE

Numerical optimization of threshold voltage and off-current of a nano-scale symmetric double gate MOSFET based on the genetic algorithm: Various strategies compatible with device applications

Yazdan Karimi Pashaki¹, Seyed Ali Sedigh Ziabari^{1, *}, Abdollah Eskandarian¹, Ali Rahnamaei²

¹ Department of Electrical Engineering, Rasht Branch, Islamic Azad University, Rasht, Iran ² Department of Electrical Engineering, Ardabil Branch, Islamic Azad University, Ardabil, Iran

Received 22 July 2022; revised 07 November 2022; accepted 12 November 2022; available online 19 November 2022

Abstract

In this paper, we optimize the electrical characteristics of Nano-scale symmetric double-gate metal oxide semiconductor field effect transistors (DG-MOSFETs) for digital applications using a genetic algorithm. We use a single-objective genetic algorithm to optimize the threshold voltage (V_{th}) with a distinct analytical relationship. The optimization of the threshold voltage is accomplished for three cases with considering two structural variables of the oxide thickness (t_{ox}), the channel thickness (t_{si}), and the channel doping density (N_a). The fourth case of optimization is done with considering these three variables. Comparison of these four cases illustrates that the best threshold voltage is 0.15 V for a channel doping concentration of 1.2×10^{-10} cm⁻³ and an oxide thickness of 1.49 nm. In addition, we optimize the OFF-current criterion based on the gate oxide thickness, the channel thickness, the channel doping concentration and the channel length and width. The optimization processes of the device are validated by simulating in SILVACO software. Furthermore, we use the two-objective genetic algorithm with the threshold voltage and the OFF-current objects for four structural variables including the gate oxide thickness, the channel layer thickness, and the channel length and width. This process is applicable to digital circuit design. To evaluate the accuracy of the proposed device optimization, the optimized device and other situations are simulated in SILVACO simulator. The optimized device illustrates the best treatment.

Keywords: Genetic Algorithm; Nano-Scale Double-Gate MOSFET; OFF-Current; Scaling; Threshold Voltage.

How to cite this article

Karimi Pashaki Y., Sedigh Ziabari S.A., Eskandarian A., Rahnamaei A. Numerical optimization of threshold voltage and offcurrent of a nano-scale symmetric double gate MOSFET based on the genetic algorithm: Various strategies compatible with device applications. Int. J. Nano Dimens., 2023; 14(1): 91-102.

INTRODUCTION

The downscaling of device dimensions has been the primary factor to improve integrated circuits performance and power efficiency [1]. In the age of modern VLSI industry, cost-effective and high-performance semiconductor devices have a considerable role in circuit design. To achieve an efficient device, the dimensions of MOSFETs have been continuously reduced to the nanometer range [2-4]. Focusing on the downscaling of transistors leads to the improvement of the efficiency and developing the semiconductor industry consisting of the nanotechnology in the device design reduces

an I_{ON} [9]. Recently, multiple gate MOSFETs, such as the double MOSFET, the omega MOSFET, the gate all around (GAA) MOSFET, and quadruple-shape MOSFETs have been introduced as promising substitutions for the conventional MOSFET to suppress the scaling limitations [10-11]. The various structures of double-gate MOSFETs are significant structures to design CMOS circuits,

power consumption and cost [5]. Conventional

field effect transistors (FETs) have high-level static

power dissipation, limited sub-threshold swing,

and switching speed [6-8]. The design methods

of advanced MOSFET have presented high

performance Nano-scale devices with good I OFF and

* Corresponding Author Email: *sedigh@iaurasht.ac.ir*

Copyright © 2023 The Authors.





Fig. 1. The cross-sectional view of symmetric DG-MOSFET [25].

therefore, designing these devices in Nano-scale can be important [12-14]. Various simulations and optimization approaches have been accomplished to decrease the limited behaviors of the scaling and short channel effects [15-16]. To improve the device performances for analog or digital applications, design approaches based on the evolutionary algorithms can be effective to advance the appropriate scaling of devices [17]. The genetic algorithm (GA) is an important method for identifying optimal solutions to difficult problems. It has been constructed based on the evolution and natural selection [18]. This algorithm is suitable to determine the different parameters of a FET to optimize main characteristics [19-22]. In the device optimization process, the objective functions are determined based on analytical models of the device. Double-gate MOSFETs (DG-MOSFETs) are the significant choice for very large scale integrated (VLSI) technology [23]. We use the results of analytical model, which is based on solving the Poisson equation and current correlation equations without charge-sheet approximation [24], to obtain the main characteristics of DG-MOSFET and then optimize them based on different device parameters.

MATERIALS AND METHODS

The cross-section of symmetric double-gate MOSFET is shown in Fig. 1 [25]. The length and width of the gate are 18 μ m and 1.2 μ m, respectively. The n-type doping concentration of the source and drain regions are 10^{20} cm⁻³ and the p-type doping of the channel is assumed 10^{13} cm⁻³. In this paper, we

use the genetic algorithm to optimize the threshold voltage and OFF-current of the device based on variation of the main parameters such as the oxide thickness, the channel layer thickness, the channel length, the gate width and the channel doping concentration. One of the important electrical characteristics described by the analytical model of the FET illustrated in Fig. 1, is the threshold voltage. It is calculated based on a charge-sheet model to solve the 1-D Poisson equation [25]. The Poisson equation is solved in the x-direction, along the axis from the gate to the channel. The Poisson equation shown below is solved one-dimensionally to determine the surface and central potentials [25].

$$\frac{d^2\phi}{dx^2} = \frac{q}{\epsilon_{si}} \left[\frac{n_i^2}{n_a} e^{(\phi - v_{ch}/v_t)} + n_a - n_a e^{(-\phi/v_t)} \right]$$

 $\mathbf{\phi}$ is the electrostatic potential, which is a function of x, and the surface and central potentials are the same as the φ potential at the points $x = t_{si}/2$ and x = 0. Where n_i is the carrier concentration, n_a is the uniform acceptor doping concentration in the channel, q is the electron charges, $\boldsymbol{\varepsilon}_{si}$ the dielectric permittivity of Si, V_{ch} is the electron quasi-Fermi potential, V_t is the thermal voltage. Based on the solutions of $\boldsymbol{\varphi}_{s}$ and $\boldsymbol{\varphi}_{0}$, the combination of the 1-D Poisson equation, Gauss law, and Boltzmann distribution, the analytical threshold voltage is obtained using the following equation [25]

(1)

$$V_{th} = V_{fb} + V_t ln\left(\frac{2n_a^2}{n_i^2}\right) + \frac{qn_a t_{si} t_{ox}}{\varepsilon_{ox}} + 3V_t$$



Fig. 2. (a) Variations of objective function (b) V_{tb} versus the doping concentration and the channel thickness.

To optimize the threshold voltage of the transistor, we consider V_{th} in equation (2) as the objective function in the genetic algorithm and the oxide thickness, the silicon layer thickness (channel thickness), and the channel doping concentration as variables. Another important electrical characteristic of MOSFET is the OFF-current. The drain-source current is modeled with a gradual-channel approximation based on the charge-sheet in the channel, which is expressed as follows [25]

$$I_{ds} = \mu C_{ox} \frac{W}{L} \Big[-\phi_{s}^{2} + 2(V_{gs} - V_{fb} - \frac{qN_{a}t_{si}}{2C_{ox}} + V_{t})\phi_{s} \Big] \frac{\phi_{ss}}{\phi_{sd}}^{(5)}$$

Where, φ_{ss} and φ_{SD} are the solutions of φ_s at the source and drain terminals as $V_{ch} = 0$ and $V_{ch} = V_{DS}$ respectively. According to equation (3), at $V_{GS} = 0$ V the OFF-current is achieved. Therefore, to optimize this factor as the objective function in the genetic algorithm, the gate oxide thickness (t_{ox}) , the channel thickness (t_{si}) , the channel doping concentration (N_a) , and the channel length and width are variables.

RESULTS AND DISCUSSION

Single-objective multivariable optimization procedure with genetic algorithm

In the double-gate MOSFET optimization process, a single-objective multivariable genetic algorithm is used to optimize the threshold voltage and OFF-current. The general optimization process with a genetic algorithm is performed by determining the vector of decision variables, generating the initial population, selecting the type of genetic operators and evaluating the device variables to obtain acceptable values of the objective functions. During the optimization process, the generation criterion for determining new offspring with mutation and crossover operators is changed



Fig. 3. (a) Variations of objective function with iteration, and (b) V_{th} versus the doping concentration and the oxide thickness.

Int. J. Nano Dimens., 14 (1): 91-102, Winter 2023

Y. Karimi Pashaki, S.A Sedigh Ziabari, et al.



Fig. 4. (a) Variations of objective function with iteration, and (b) V_{th} versus the channel and the oxide thickness.

and evaluated [26].

The threshold voltage optimization based on the oxide thickness, the channel thickness and the channel doping concentration variables

In this section, the threshold voltage optimization is performed in four independent states using the single-objective genetic algorithm, and the results are compared in these states. In the first state, the doping concentration and the channel thickness variables are used to optimize the threshold voltage, while the oxide thickness is assumed to be 2 nm. Fig. 2(a) illuatrates V_{th}versus the generation of the algorithm and Fig. 2(b) shows V_{th} versus the doping concentration and the channel thickness. As can be seen in Fig. 2(b), the optimized value of the threshold voltage is 0.19 V for a channel thickness of 14.48 nm and doping concentration of 2.3×10^{10} cm⁻³. Fig. 2(a) shows the variation in threshold voltage with generation for a maximum iteration of 400 and an initial population of 200.

The density of the impurity is approximately equal to the intrinsic density of the channel according to equation (2), and the flat band voltage is zero. In the second state, the channel doping concentration and the gate oxide thickness are assumed to be variables, and the channel thickness is 10 nm. In Fig. 3(a), the threshold voltage variations versus generations of the algorithm are shown. Fig. 3(a) shows that the optimum threshold voltage at 92 iterations is 0.15 V. The optimal threshold voltage is achieved for the channel doping concentration of 1.2×10¹⁰ cm⁻³ and an oxide thickness of 1.49 nm. This amount of the channel doping concentration is approximately similar to the intrinsic channel. Fig. 3(b), shows the optimized value of the threshold voltage versus the doping concentration and the oxide thickness. In the third stage, the threshold voltage is optimized by varying the oxide thickness and the channel thickness, and a constant value of the doping concentration. Fig. 4(a) indicates the optimal value of the device threshold voltage versus



Fig. 5. Calibration of simulation results and reported data in [25].



Fig. 6. I_{DS}-V_{GS} characteristics for nano-scale double-gate MOSFET versus the channel thickness.

the number of iterations. Fig. 4(b) shows V_{th} versus the oxide thickness and the channel thickness. The optimized threshold voltage is 0.273 V achieved by $t_{i} = 0.84$ nm and $t_{i} = 11$ nm. This strategy is not appropriate and applicable as optimization method because of small variation in V_{th}. In the fourth stage, the genetic algorithm optimizes the threshold voltage for three variables including the oxide thickness, the channel thickness, and the channel doping concentration. The results of optimization of the single-objective genetic algorithm by simultaneously changing these three variables are shown in Table 1. As it can be seen in this table, the optimized threshold voltage is 0.29 V for $t_{ov} = 1.82$ nm, $t_{si} = 17.5$ nm and $N_{a} = 1.5 \times 10^{10}$ cm⁻³. The results of the single-objective algorithm can be validated by SILVACO simulation. Initially, we are calibrated the SILVACO software simulation using the results reported in [25]. Fig. 5, shows that our simulation results has appropriate accordance with the results of [25] for a distinct double-gate MOSFET. We used the calibrated simulation to validate the optimization results. The simulation results of SILVACO for different values of the channel thicknesses are shown in Fig. 6. This figure shows the drain-source current versus gate-source voltage for four different channel thicknesses. The optimized device has the minimum V_{th} compared to the others, including the device in [25]. The optimized results of the double-gate MOSFET threshold voltage for the four cases of optimizations described above are presented in Table 2. According to this table, the optimum threshold voltage value is 0.15 V for the case 2. In this case, the oxide thickness and the channel doping concentration are assumed to be variable, and the channel thickness is constant. The optimum oxide thickness and channel doping concentration are 1.49 nm and 1.2×10¹⁰ cm⁻³, respectively. Therefore, we can select the best strategy based on a comparison of the four cases.

Optimization of the double-gate Nano-scale MOSFET OFF-current with multivariable singleobjective genetic algorithm

Based on equation (3), the single-objective

Table 1. Optimized nano-scale symetric double-gate MOSFET parameters.

Parameter	Description	Optimized Design
$egin{array}{c} t_{ m ox} \ t_{ m si} \ N_a \ V_{ m th} \end{array}$	Oxide thickness Channel thickness Channel doping concer Threshold voltage	$\begin{array}{c} 1.82 \text{ nm} \\ 17.5 \text{ nm} \\ 1.5 \times 10^{10} \text{ cm}^{-3} \\ 0.29 \text{ V} \end{array}$

Optimization cases	case 1	case 2	case 3	case 4	
Threshold Voltage (V _{Th})	0.19 V	0.15 V	0.273 V	0.29V	

Table 2. Optimized double-gate MOSET design characteristic.

Table 3. Optimized Nano-scale symetric DG-MOSFET design parameters versus V_{DS} = 1 v.

Parameter	Description	Optimized Design
t _{ox}	Oxide thickness	2.33 nm
t _{si}	Channel thickness	21.44 nm
W	Channel width	40 nm
L	Channel length	70.85 nm
N_a	Channel doping	$1.36 \times 10^{10} \text{ cm}^{-3}$
Ioff	OFF- current	3.97× 10 ⁻¹¹ A

genetic algorithm optimizes the OFF-current for five variables of the device, including the gate oxide thickness, the channel thickness, the channel doping concentration, and the channel length and width. The drain-source voltage is assumed to be 1 V. Fig. 7, shows the optimal amount of the OFF-current for a population iteration of 300 and apopulation size of 200. According to Fig. 7, the amplitude of the current reached its minimum stable value at iteration 38. It can be seen in table 3 that the calculated optimal value of the OFFcurrent is 3.97×10^{-11} Å achieved based on five variables. The drain-source current versus the gatesource voltage of the optimized device described in Table 3 is simulated in SILVACO, as illustrated in Fig. 8. The OFF-current shown in this figure and table 3 are identical. The optimized device can be evaluated by simulation using SILVACO. Fig. 9 illustrates the simulated device characteristics for the different channel thicknesses. The OFF-current of the optimized device is compared with that of in other situations. It is obvious that lowest OFFcurrent for the different values of t_a is obtained for our optimized device shown in Table 3. Therefore, the optimized device is validated based on the channel thickness parameter. The current-voltage characteristics of the device simulated by SILVACO for different oxide thicknesses are shown in Fig. 10. According to Fig. 10, the OFF-current in the optimal state has the best value compared with that of different values of the oxide thickness. Moreover, we have simulated the transistors for different



Fig. 7. I_{DS} versus the iteration of algorithm.

Y. Karimi Pashaki, S.A Sedigh Ziabari, et al.



 $\label{eq:Gate-to-Source Voltage, V} Gate-to-Source Voltage, V_{GS} \ensuremath{\left[V\right]}\xspace$ Fig. 8. $I_{\rm DS}\text{-}V_{\rm GS}$ characteristics simulated with SILVACO for optimized design.



Fig. 9. I_{DS}-V_{GS} characteristics for different channel thicknesses and comparison with the optimized device.

channel lengths using SILVACO, as shown in Fig. 11. This figure shows that the optimzation of the device is true. In this work, the OFF-current and threshold voltage of the Nano-scale double-gate MOSFET have been optimized separately using a the single-objective genetic algorithm for the device variables. The optimization results have been evaluated and validated using the SILVACO simulation. Based on the results, we have optimized the reference device [25]. In the next section,

the OFF-current and threshold voltage will be optimized simultaneously using a two-objective genetic algorithm.

OFF-Current and Threshold Voltage Optimization with Two-Objective multivariable Genetic Algorithm

In the previous sections, the OFF-current and threshold voltage were separately optimized using a single-objective genetic algorithm. In some device applications such as digital circuits design





Fi. 10. I_{DS}-V_{GS} characteristics for different oxide thicknesses and comparison with the optimized device.

the two-objective optimization is necessary. In this study, multi-objective optimization is performed using the NSGA-II method, and NSGA algorithm proposed by Deb in 1994 [27-28]. In this section, we optimize the OFF-current and threshold voltage simultaneously. The variations in the oxide thickness, channel thickness, and channel length and width were used as variables for the two-objective genetic algorithm in the process of simultaneously optimizing the threshold voltage and OFF-current. The Fig. 12 shows the optimization of the threshold voltage and OFF-current of the device using the two-objective Pareto genetic curve. Fig. 12 shows the optimal values of the threshold voltage and the OFF-current. According to this figure, the threshold voltage and the OFF-current at the specified point of the graph have minimum values. The channel doping concentration is a fixed value of 4×10^{12} cm⁻³, the population size is 65 and the number of iterations is 170. The optimized results of the threshold voltage and the OFF-current using the two-objective genetic algorithm are presented in Table 4. At this state, to confirm the optimized characteristics, we simulate the device based on the specifications contained in Table 4 by SILVACO. The I_{DS}-V_{GS} is shown in Fig. 13. According to Fig. 13, the optimized results of the threshold voltage and the OFF-current are confirmed by SILVACO. Fig. 14





Fig. 12. Pareto front diagram for the optimized objective functions, $(I_{DS}-V_{th})$.

shows the I_{DS} -V_{GS} characteristics of the optimized device, as shown in Table 4. The simulation results for different oxide thicknesses are illustrated in this figure. It can be observed that the optimum device has the best OFF-current and threshold voltage, simultaneously. Fig. 15 shows the Nano-scale device simulation using the SILVACO for different channel thicknesses. The variation in the channel thicknesses causes to destroy the simultaneous optimization of the OFF-current and V_{th}. Next state, we are performed simulations for different channel lengths. Fig. 16 illustrates the results of the device simulation for different channel lengths. With increasing channel length, the amount of OFFcurrent is increased and V_{th} is decreased. Therefore, the channel length in other values compared with that of the optimized situation causes to damage the simultaneous optimization of device.

CONCLUSION

We have optimized the threshold voltage and the OFF-current of a Nano-scale symmetric double-gate MOSFETs for digital applications by the genetic algorithm. We have used the singleobjective genetic algorithm to optimize the threshold voltage. This optimization has been done for four cases based on different structural variables. The optimized value of threshold voltage were 0.19 V for $t_{si} = 14.48$ nm and $N_a = 2.3 \times 10^{10}$ cm⁻³, 0.15 V for $N_a = 1.2 \times 10^{10}$ cm⁻³ and $t_{ox} = 1.49$ nm, 0.273 V for $t_{ox} = 0.84$ nm and $t_{si} = 11$ nm, and 0.29 V for three parameters of $t_{ox} = 1.82$ nm, $t_{si} = 17.5$ nm and $N_a = 1.5$



 $\label{eq:Gate-to-Source Voltage, V_{GS} [V]} Fig. 13. \ I_{\rm ns} \text{-} V_{\rm GS} \ characteristics simulated with SILVACO for optimized design for two-objective genetic algorithm.}$

Int. J. Nano Dimens., 14 (1): 91-102, Winter 2023

Y. Karimi Pashaki, S.A Sedigh Ziabari, et al.

Parameter	Description	Optimized Design	
t _{Ox}	Oxide thickness	2 nm	
t _{Si}	Channel thickness	12.44 nm	
W	Channel width	20.0 nm	
L	Channel length	50.0 nm	
I _{OFF}	OFF-state current	1.49×10 ⁻¹¹ A	
V_{Th}	Threshold voltage	0.389 V	

Table 4. Optimizing the OFF-current ($V_{DS} = 1 \text{ V}$ and $V_{GS} = 0.0 \text{ V}$) and threshold voltage.



 $Gate-to-Source\ Voltage,\ V_{GS}\ [V]$ Fig. 14. $I_{_{DS}}\text{-}V_{_{GS}}$ characteristics for different oxide thicknesses and comparison with the optimized device.



Gate-to-Source Voltage, VGS [V] Fig. 15. I_{DS} - V_{GS} characteristics for different channel thicknesses and comparison with the optimized device.



Gate-to-Source Vpltage, V_{GS} [V] Fig. 16. I_{DS} - V_{GS} characteristics for different channel lengths.

×10¹⁰ cm⁻³. The optimal threshold voltage was 0.15 V for the second proposed case including variables of N_a and t_{ox}. Moreover, the optimized OFF-current has been calculated 3.97×10^{-11} A for t_{ox}=2.33 nm, t_{si}=21.44 nm, W=40 nm, L=70.85 nm, and N_a=1.36 ×10¹⁰ cm⁻³. The optimization processes have been validated by the simulation of optimized devices and other situations in SILVACO software. Finally, based on simultaneous optimization, the threshold voltage and the OFF-current have been calculated 0.389 V and 1.49×10⁻¹¹ respectively, for t_{ox}= 2 nm, t_{si}= 12.44 nm, W= 20 nm, and L=50 nm. The accuracy of the proposed device optimization has been assessed by simulating the optimized device and other situations in SILVACO software.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

REFERENCE

- Elmessary M. A., Nagy D., Aldegunde M., Seoane N., Indalecio G., Lindberg J., Dettmer W., Peric D., García-Loureiro A. J., Kalna K., (2017), Scaling/LER study of Si GAA nanowire FET using 3D finite element Monte Carlo simulations: Scaling limits and opportunities. *Solid-State Electronics*. 128: 17-24.
- Choi W. Y., Park B. G., Lee J. D., Liu T. J. K., (2007), Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60mV. *IEEE. Elec.* 28: 743–745.
- Ebrahimnia M., Sedigh Ziabari S. A., Kiani-sarkaleh A., (2022), Influence analysis of dielectric pocket on ambipolar behavior and high-frequency performance of dual material gate oxide stack-double gate Nano-Scale TFET. J. Nanoanalysis. Articles in Press.
- 4. Vimala P., Balamurugan N. B., (2013), Modelling the centroid and charge density in double-gate MOSFETs

 including quantum effects. Int. J. Elec. 100: 1283-1295.
 Ratnesh R. K., Goel A., Kaushik G., Garg H., Chandan., Singh M., Prasad B., (2021), Advancement and challenges in MOSFET scaling. Mater. Sci. Semi. Proc. 134: 106002.

- Ionescu A. M., Riel H., (2011), Tunnel field-effect transistors as energy-efficient electronic switches. *Nature*. 479: 329-337.
- Anghel C., Chilagani P., Amara A., Vladimirescu A., (2010), Tunnel field effect transistor with increased on current, low-k spacer and high-k dielectric. *AIP. Applied. Phys. Let.* 96: 122104-1-3.
- Cristoloveanu S., Wan J., Zaslavsky A., (2016), A Review of sharp-switching devices for ultra-low power applications. *IEEE. J. Elec. Dev.* 4: 215-226.
- Aditya M., Srinivasa-Rao K., (2021), Design and performance analysis of advanced MOSFET structures. *Trans. Elect. Electronic Mat.* 23: 219-227.
- Ferain I., Colinge C. A., Colinge J. P., (2011), Multigate transistors as the future of classical metal-oxidesemiconductor field-effect transistors. *Nature*. 479: 310-316.
- 11. Sun Y., Yu U., Zhang R., Chen B., Cheng R., (2021), The past and future of multi-gate field-effect transistors: Process challenges and reliability issues. *J. Semi.* 42: 023102.
- Anthony-Uchechukwu M., M-Srivastava V., (2020), Channel length scaling pattern for cylindrical surrounding double-gate (CSDG) MOSFET. *IEEE Access.* 8: 121204-121210.
- Sze M., (2002), Physics of semiconductor devices. Wiley-Inter science.
- Kumar K., Khiangte L., Sankar-Dhar R., (2020), Design of DG MOSFET with tri-layered strained silicon channel. J. Physics: Conf. Series. 1478: 012002.
- Coquan R., Casse M., Barraud S., Cooper D., Alvaro V. M., Samson M. P., Mofray S., Boeuf F., Ghibaudo G., Faynot O., Poiroux T., (2012), Strain-induced performance enhancement of tri-gate and omega-gate nanowire FETs scaled down to 10 nm width. *IEEE*. 60: 727-732.
- Khan A., A-Loan S., (2020), Metal drain double-gate tunnel field effect transistor with underlap: Design and simulation. *Silicon.* 13: 1421-1431.



- Djeffal F., Abdi M. A., Dibi D., Chahdi M., Benhaya A., (2008), A neural approach to study the scaling capability of the undoped double-gate and cylindrical gate all around MOSFETs. *Mater. Sci. Eng.* 147: 239-244.
- Giuseppe A., Butera F., Nella R., (2014), Geometrical and physical optimization of a photovoltaic cell by means of genetic algorithm. *J. Compu. Electron.* 13: 323-328.
- Parvane M., Rahimi E., Jafarinejad F., (2020), Optimization of quantum cellular automata circuits by genetic algorithm. *Int. J. Eng.* 33: 229-236.
- Liu W., Jin X., Xi X., Chen J., Jeng M., Liu Z., Cheng Y., Chen K., Chan M., Hui K., Huang J., Tu R., Ping-Ko K., Hu C., (2005), User's Manual. Dep. Ele. Eng. Compu. Sciences. University of California, Berkeley.
- McCall J., (2005), Genetic algorithms for modelling and optimization. J. Comput. Appl. Mathem. 184: 205-222.
- 22. Suzuki K., Takai N., Sugawara Y., Kato M., (2017), Automatic design of operational amplifier utilizing both equation-based method and genetic algorithm. *IEICE*.

Trans. 100: 2750-2757.

- Frank D. J., Dennard R. H., Nowak E., Solomon P. M., Taur Y., Wong H. S., (2001), Device scaling limits of Si MOSFETs and their application dependencies. *IEEE*. 89: 259-288.
- Taur Y., Liang X., Wang W., Lu H., (2004), A continuous, analytic drain-current model for DG MOSFETs. *IEEE. Elec. Dev. Lett.* 25: 107-109.
- Yu F, Huang G., Lin W., Xu C., (2018), An analytical drain current model for symmetric double-gate MOSFETs. *AIP. Adv.* 8: 045125: 1-11.
- Marseguerra M., Zio E., Cipollone M., (2003), Designing optimal degradation tests via multi-objective genetic algorithms. *Reliability. Eng. Sys. Safety.* 79: 87-94.
- Srinivas N., Deb K., (1994), Multi-objective optimization using non-dominated sorting in genetic algorithms. *IEEE. Evolutionary. Comput.* 2: 221-248.
- Deb K., Grawal S. A., Pratap A., Meyarivan T., (2002), A fast and elitist multi-objective genetic algorithm: NSGA-II. IEEE. *Trans. Evolutionary. Comput.* 6: 182-197.