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ORIGINAL ARTICLE

A low-power, wideband-tunable, nano-dimension based CMOS LC ladder filter designed using GmC

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Abstract

This paper proposed LC-ladder filter based on transconductance (GmC) with 130 nm RF CMOS process technology node at 1.2 V. Further, a seventh-order low-pass filter prototype and a sixth-order band-pass filter prototype have been invented to prove high-frequency functioning in a way that is relatively suited for s-parameters modelling. The low pass and band pass elements of an LC filter have been successfully implemented with GmC, and high-frequency operation has been achieved with compact passive components. To perform simulations and validate s-parameters in the intended frequency range of 2 GHz to 6 GHz, an RF-simulation platform (ADS from Keysight) has been utilised. The 8-bit capacitor-bank array used in this device allows the wideband adjustable function to be controlled by a digital or analogue signal from the external control. Due to the current mode multi-port GmC operation, an average selectivity with Q in the range of 27 to 39 has been achieved at 4.3mW, while maintaining low power consumption. By selecting the appropriate Gm and capacitive sizes for the cap-bank, it was feasible to achieve the broad operation required in the existing wireless range (2GHz-6GHz). SPICE and RF (s-parameter, harmonic balancer) simulations in ADS have been used in combination to examine the frequency response and noise performance of the proposed structure. When compared to state-of-the-art-work, the suggested Low power tunable filter stands out because to its improved frequency range, low supply voltage, better value of noise performance, and low power dissipation, which will be useful for complex analogue circuit design.

Keywords: *ECircuit; CMOS; Filter; GmC; Inductor Emulation; Nano-Dimension; Signal Processing.*

How to cite this article

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INTRODUCTION

In wireless communication systems, the received signal is determined by the radio receiver's capacity to pick up the signal as it is being broadcast over the radio channel. This capability is dependent on the radio receiver [1]. The most important function of a radio receiver is signal amplification and filtering. Amplification and subsequent filtering of the amplified signal are the two primary methods of signal processing that are used extensively in radio receivers. The signal is amplified first, and then it is filtered after it has been amplified. These two steps are instances of signal processing. These two supporting operations are often dispersed throughout many distinct receiver blocks since this is the most efficient use of space. A flat frequency response is often sought because wideband wireless applications sometimes demand that the frequency response of a receiver chain be flat for in-band transmissions. This is one of the reasons why a flat frequency response is desired in general. As a consequence of this, out-of-band signals and adjoining channels need to be suppressed to a sufficiently low level so that the bit error rate of the receiver is not negatively impacted by them [2].

To make the most efficient use of the space that is available, these two supporting activities are frequently dispersed throughout a variety of receiver blocks [2]. This is the approach that

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is proven to be the most effective. When it comes to receiver chains, a smooth frequency response is very desirable because it allows for in-band transmissions in wideband wireless applications. Because of this, a flat frequency response is frequently one of the most sought-after characteristics of a receiver chain. This particular advantage is one of the reasons why a flat frequency response is necessary for general since it is one of the reasons why a flat frequency response is essential. Therefore, out-of-band signals and channels that are adjacent to the one being received must be suppressed to a sufficiently low level so that the bit error rate of the receiver is not negatively affected [3]. This can be accomplished by setting the level of suppression to a sufficiently low value. This can be performed by adjusting the degree of suppression to a value that is low enough to meet the requirements. It is vital to utilise selective analogue baseband low-pass filtering that features an exceptionally low pass-band ripple in a wide variety of applications because this type of filtering is required. On the other hand, this specific form of filtering is of the utmost significance in low-IF receivers and direct-conversion receivers respectively. This is because low-IF receivers and direct-conversion receivers receive their signals directly. However, due to the imperfect nature of the integrated active devices used to build the filter, the frequency response's shape might quickly deteriorate. This is because the filter is composed of integrated active devices. This is something that could happen given that the filter is built out of active electronics that are integrated into its construction. This unanticipated outcome is made a great deal more problematic by the requirement, which must be satisfied, that a sizeable amount of bandwidth is made available. One of the main goals of the offered research is to ascertain whether or not exact frequency response shapes may be realised in typical ultra-deep-submicron CMOS technology for integrated wideband continuous-time low-pass filters. The feasibility of integrating high-pass filters with conventional ultra-deep-submicron complementary metal-oxide-semiconductor (CMOS) technology is also a key focus of the studies described here. This is a result of the factors that were discussed earlier. This is because the production of many modern electronic gadgets necessitated the incorporation of these filters as a necessary component. CMOS technology with a 65nm process is utilised in the construction of this design.

Utilizing a baseband filter in the context of analogue signal processing permits the selection of channel filtering that is unique to the signal that is being processed. This is possible thanks to the versatility of baseband filters. The receiver node is the location where passive filtering is performed, and the filter that is created as a result of this process possesses a certain quality such as selectivity. If the signal is going to be transmitted through the system, the design of the system will determine how the signal will be partitioned, and the characteristics of the signal will be characterised by the system blocks if the signal is going to be transmitted through the system. In addition, how the signal will be transmitted will be established by the design of the system. The type of filter that is integrated into the system can function in either continuous time or discrete time; the mode of operation that is picked is determined by the criteria that are posed by the user. When we take into account the speed factor of continuous-time filters, which is an advantage, as well as the fact that discrete-time filters do not require sampling, we find that both continuous and discrete filters have their distinct advantages. One of these advantages is the speed factor of continuous-time filters. When it comes to wideband applications, the continuous time filter is the one that is recommended to be used, since it is the one that offers the best performance. It is discussed in reference [4] how the architecture of the chip incorporates the utilisation of a WCDMA channel that is comprised of several carriers. WCDMA of the single-chip level with multi-carrier types of signals is going to be studied, and the reference [5] is going to include detailed simulation results. You can find a presentation on the pre-distortion category known as gm-C type filters by consulting reference [6]. This particular type of filter makes use of a specific trans-conductance and possesses a DC gain that is adjustable by the user. Every single one of the designs being developed makes use of the CMOS process technology in some way. The results of implementing this design with a single-level chip in the context of a WiMedia UWM type receiver are presented in the aforementioned reference [7].

These days, designs of the ABB type are more widespread since they are applicable to a broad variety of fields, cellular-type networks [8-13],

such as radar applications [12], and radio receivers [8-13]. There is a data limitation in the application of the ABB type design that was just discussed [14-20]. When it comes to the communication system, speed is the one component that stands out as being crucial for an advanced system [20-25]. In the article that is referred to as [26], it is discussed how the design of ABB architecture helps to increase energy efficiency and scalable power. Additionally, an ABB type design with a full analysis is presented and discussed. Both of the styles of design that have been discussed thus far make use of a particular goal or objective. According to the information presented in references [15-17], the architecture of the design makes use of a great deal of sub-type circuits.

It is possible to select the filtering characteristics of a particular channel by making use of a baseband filter as part of the framework of analogue signal processing. The receiver node is the one that is in charge of carrying out the process of passive filtering, and the filter that is created as a direct result of this process possesses a certain quality such as selectivity. If the signal is going to be transmitted through the system, the design of the system will determine how the signal will be partitioned, and the characteristics of the signal will be characterised by the system blocks if the signal is going to be transmitted through the system. If the signal is going to be distributed across the entirety of the system, the architecture of the system will also decide how the signal will be segmented. The kind of filter that is used in the system can function in either continuous time or discrete time; the mode of operation that is used is determined by the needs of the user. If we take into account the speed factor of continuous-time filters, which is an advantage, as well as the fact that discrete-time filters do not require sampling, then it can be said that both continuous and discrete filters have their distinct advantages [1-3]. Any application that necessitates wideband performance ought to make use of the continuous-time filter. This is the filter that ought to be used. In the design of the semiconductor that is described in reference [4,] we make use of a WCDMA channel that is composed of multiple carriers. Discuss the WCDMA type that operates at the single-chip level and offers thorough simulation results in the reference [5]. This WCDMA type makes use of numerous carriers to transmit various types of signals. In reference [6] the pre-distortion category that is commonly referred to as the gm-C type filter was discussed. This collection of filters makes use of a certain trans-conductance, and its DC gain can be adjusted according to the user's preferences. Every single design utilises CMOS technology, which is a form of processing. This is the case for all of them. In reference [7], the results of implementing this design using a single-level chip in the context of a WiMedia UWM-type receiver are described. The CMOS technology with a 65nm process has been included in this design. Existing designs of low-power tunable filters are flawed in many different aspects, such as power dissipation, noise performance, a key component of wideband adjustable coverage, and so forth. New designs are needed to address these issues and others. This article offers a low-power adjustable filter as a potential solution to these issues so that they can be circumvented in the future. The performance of the filter that was already in place was compared to that of the tunable filter that was described, and both the positive and negative features of both filters were outlined and explained.

The most significant findings and insights presented in this article are as follows:

- The method for designing a GmC-based current mode LC ladder filter suitable for 130nm-RF CMOS Technology with a wideband tuning feature has been proven in this study.
- The parameters are analysed and evaluated, including power dissipation, noise performance, frequency range and filter order.
- When compared to other tuning filters existing in the literature, the performance parameters of this tuning filter stand are superior.

The organizational components of this paper are as follows: In Section II, an attempt has been made to achieve the desired operation by utilizing the fundamental LC ladder architecture. The band of operation that is desired is S and C for present WLAN applications. The GmC-based implementation strategies are broken down into even more specifics in Section III of the document. The findings of the simulation are provided in Section IV, and a conclusive proposal for the development of a switchable filter that is suitable for the aforementioned application range has been presented. In addition to this, the results of the simulation are compared to those obtained from previous research. In the final section, a variety of findings are broken down and analysed in further depth.

LADDER STRUCTURE DESIGN

In this section, we showed the 7th order LC ladder construction, validation results of the LC ladder, and 6th order LC ladder implementation design with validation results using ADS simulator. There are two main methods such as cascaded biquads and lossless doubly terminated LC ladder implementation used to synthesize higher-order filters, and both are explained in this section. Both of these implementations are known as cascaded biquads. The cascaded biquad is utilized significantly more frequently than the other filters. The majority of applications favour the lossless doubly terminated LC ladder method rather than the cascaded biquads method. Cascaded biquads are the alternative way. This is as a result of the fact that it generates filter realizations that are tolerant to component fluctuation, that it has a substantially greater dynamic range of performance, and that it has significantly enhanced pass-band magnitude response accuracy. This advantage over cascaded biquads is a result of the fact that the lossless doubly terminated LC ladder technique was proposed in a considerable body of research [18, 19]. This research led to the development of the lossless doubly terminated LC ladder approach. Cascaded biquads have some drawbacks, which led to the development of this approach to address those issues. In fact that this method needs to make use of a transformer is easily the most significant downside linked with it. This is because the technology cannot be implemented in the form of an IC, as doing so would be impractical in terms of the amount of space [18]. The reason for this is that doing so would be impractical in terms of the amount of space it would consume. Advancing through time is necessary for each of these possible courses of action to be taken. As part of the tactic referred to as "element substitution," inductors are switched out for gyrators to generate the effect that is wanted. This allows for the effect to be achieved. As a result of the impossibility of producing floating inductors of sufficient quality using this method, the use of this method is restricted to only applying to systems that are based on grounded inductors. The utilization of frequency-dependent negative resistance, often known as FDNR for short, is an additional method for element replacement that can be utilized. This form of resistance is one of the most common types because it is suitable for the construction of low-pass filter components and because it is one of the most common types. To simulate the interaction that takes place between varieties of passive components, the leapfrog methodology makes use of a technique that is generally referred to as a signal flow graph. This is done to create a model of how the system, in its entirety, will behave (SFG). It was necessary to use active integrators that were both lossy and lossless to bring these SFGs into the domain of the physically realizable [19]. This was necessary to shift these SFGs into this arena. The development of these filter realizations, which are known as active LC-ladder filters, is the end goal of the process that was just described.

Structure-wise, an analogue filter can be contrasted with its digital counterpart in that the analogue filter has a more traditional form. When speaking about the "structure" of an analogue filter, what is meant to be referred to is the configuration of the many components that go into making up the filter. Particular structures may turn out to be beneficial in a significant number of ways in the end. For instance, it is widespread knowledge that LC filters that operates using a ladder structure are resistant to changes in the values of their parts. This is because the ladder structure stores the values of the components in ascending order. This is because the ladder structure performs the function of a buffer for the values. The inclusion of a structure, on the other hand, makes it more difficult to find a solution to the associated design difficulty that needs to be addressed. In the field of System Design, it is a generally accepted fact that optimization strategies for design problems associated with structured systems have prohibitive computing complexity, which makes them unsuitable for application in real-world settings. This is because these strategies require an excessive amount of time and resources to solve design problems. This is a result of the fact that to put these plans into action, a considerable amount of time and money are required. As part of the standard operating procedure, the process of designing passive filters is typically divided into two stages. This is done to better organize the process. The first thing that is done is the construction of a transfer function that will be referred to later as S_{21}. The frequency response of this transfer function has a restricted range of possible values as a direct result of the modulus limitations, which has the effect of limiting the frequency response's scope. The Laplace

Table 1. List of Acronyms.

WCDMA	Wideband Code Division Multiple Access
UWB	Ultra-wideband
OTA	Operational transconductance amplifier
WLAN	Wireless Local Area Network
IC	Integrated circuit
FDNR	Frequency dependent negative resistor
SFG	Signal-flow graph
LMI	Local Management Interface
Op-amp	Operational Amplifier
LC	Tank circuit
RF	Radio frequency circuits
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
MLF	Multiple Loop Feedback
DAC	Digital to analogue converter
cap bank	Capacitor banks

transform can be used to convert the problem of synthesis into an LMI optimization problem where S_{21} is a standard transfer function that depends on the Laplace variable. This is possible because s is a variable that is associated with the Laplace transform. When s is a Laplace variable, it is conceivable for this to happen. Second, for the resultant transfer function, S21 to be reliable enough to be implemented in a specific structure, the reliability requirements that were imposed on it must first be satisfied. If these requirements are satisfied, then the resultant transfer function S_{21} will be reliable enough to be implemented. If these prerequisites are not met, the ensuing transfer function S_{21} will not be dependable enough to be put into action. Determining the restrictions placed on a generic structure can be difficult, and confirming those constraints can be an even larger issue than finding the limitations of the generic structure in the first place. On the other hand, when these strategies are put into action, they nearly never fail to yield a non-convex formulation of the problem that is being addressed. Because of this, it is vitally necessary to select an acceptable starting point to sidestep the worries surrounding convergence. This is because convergence is a phenomenon that occurs when two or more things converge. An LC-ladder filter, in which the inductances L and capacitances C are alternately set on the serial and parallel arms of the ladder filter, could seem like it would be challenging to meet these conditions. But in reality, they're not that complicated and can be simply incorporated into the LMI optimization problem necessary for s21 synthesis. This can lead one to believe that it is difficult to realize these requirements for an LC-ladder filter (Table 1).

A. *High-Frequency Applications Using an LC Ladder*

In this section, we have presented the 7th order LC ladder filter design with all validation results. The ladder network was the first generation of filters, developed in the early twentieth century before operational amplifier technology became widely accessible. This was done prior to the widespread availability of the technology necessary to operate operational amplifiers. In the early 1900s, this practice was common. The lossless is also known as the reactance ladder, is employed in situations in which op-amps are not the most effective solution. This is true even in today's modern times. This can occur because to the fact that the reactance ladder possesses a larger impedance than the lossless. If the application requires a high-frequency operation,

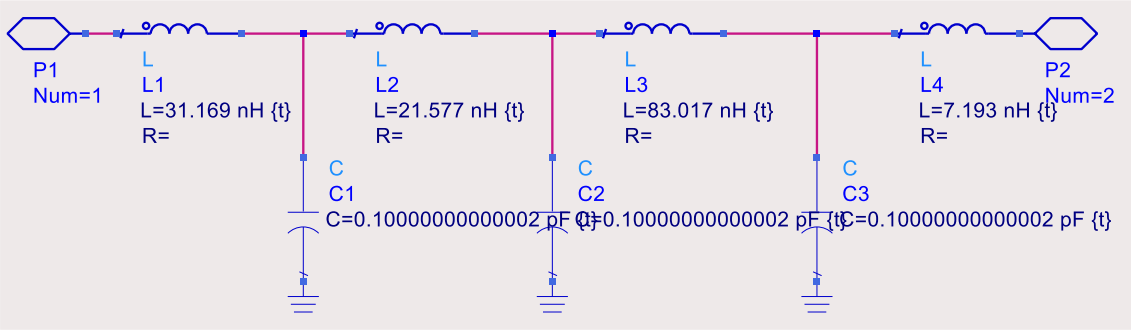
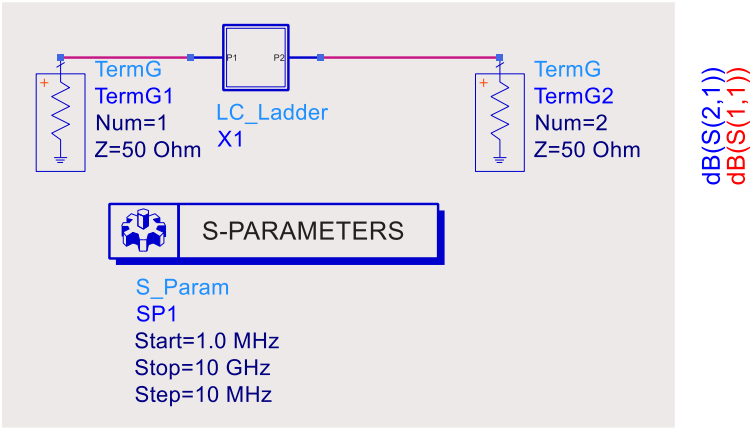


Fig. 1. A seventh-order LC for low-pass from all poles.

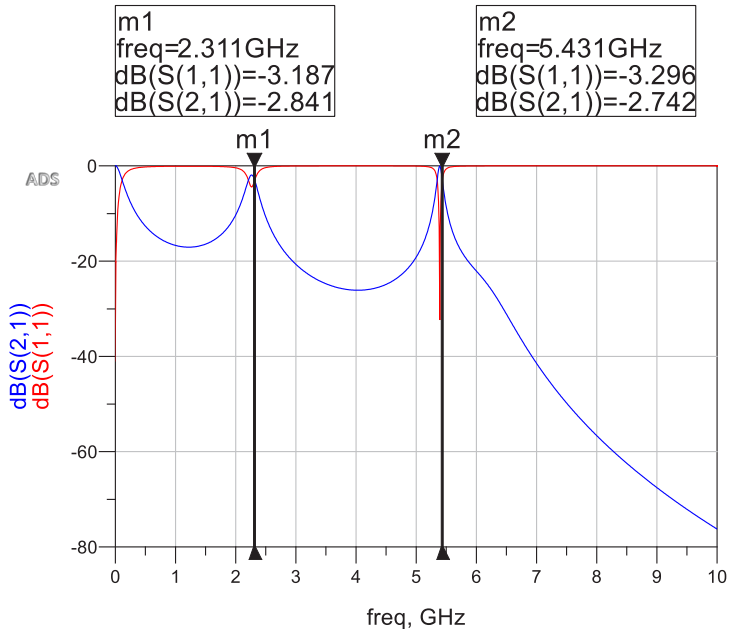
for example, or if the required power is higher than the capabilities of the op-amps or the op-capabilities, then you will need a solution that is capable of managing a higher amount of power. If the application does not require a high-frequency operation, then you do not need a solution that is capable of managing a higher amount of power. Alternatively, if the required power is more than what the op-amps are capable of handling, this could be an issue. This structure allows for the introduction of components with varied frequencies, which enables it to elicit a wide variety of responses from its audience. Because of the frequency shifts that have taken place, it is now possible to construct ladder structures that are noticeably more complex than the ones that are being exhibited here. This is because the ladder circuit displayed here is regarded to be an early model of a low-pass filter. However, it is crucial to keep in mind that each of these methods has its own particular set of benefits and that it is vital to take into consideration all of these methods.

The fundamental LC structure has a good quality factor, and the ladder that is created as a result of this structure is especially beneficial for high-frequency wideband applications. Both of these characteristics are attributable to the fact that the structure is a ladder. This is because the fundamental LC structure entails a convoluted pole insertion procedure. The vast majority of passive filters take the form of a ladder when it comes to the building of their devices, which is one of their distinguishing characteristics. It is common knowledge that ladder passive filters, which have a low sensitivity to shifts in the values of their parts, have historically been the subject of most research in the field of circuit theory. This is because ladder passive filters have a low sensitivity to shifts in the values of their parts. Ladder passive filters have a low sensitivity to fluctuations in the values of their parts, and this is the reason why this is the case. In addition, ladder filters have the advantage that all of the transmission zeros are accounted for in both the anti-resonant frequencies of the series arms and the resonant frequencies of the parallel arms of the filter structure. This is a quality that distinguishes ladder filters from other types of filters. The reason for this is that ladder filters contain arms that are organised in a configuration that is both series and parallel. The reason for this is that ladder filters contain arms that are both placed in series and arms that are arranged in parallel. This is why the situation occurs as it does. The process of filter design that is covered in this article was able to get off the ground and going because of this innate comprehension, which is explained in the article. Fig. 1 presents the conceptualization of a doubly terminated 7^{th}-order LC ladder structure. This figure also shows the functional range that this construction was built to accommodate, and it depicts those ranges (2.4GHz and 5.4GHz). The values of the shunt capacitance have been standardised to a standard range, and they have been chosen after taking into account the technology that is now available for implementation with taken proceed technology node 135nm RF-CMOS.

Figs. 2a, 2b displays the simulation setup and validation of LC ladder results that verify the aforementioned structure is the most efficient and suitable option for the proposed system. This is shown by the fact that the structure has the highest level of efficiency and also because it is the structure that is the most appropriate for the application. This may be seen by the structure having the maximum level of efficiency



(a)



(b)

Fig. 2. a) Simulation Setup for required frequency bands of WLAN (2.4GHz and 5.4GHz), b) Validation of LC ladder working in desired bands.

and also by the structure being the structure that is used for the application. Both of these aspects demonstrate that this is the case. That the frequency response was successfully obtained at the right frequency ranges is shown by the quality factor and sharper transmission factor S_{21} of the final product at those frequencies. Meaning that has been the desired frequency response was accomplished within the specified ranges. Another way of putting it is that the desired frequency response was reached at the correct frequency bands. It can also be characterised in terms of the frequency response having been produced well at the appropriate frequencies. Capacitors and inductors between 0.1 pF and 10 nH and 5 nH to 100 nH were successfully obtained. In addition to being easily attained by active implementation, this spectrum of passive elements is ideally suited with 135nm process CMOS Technology.

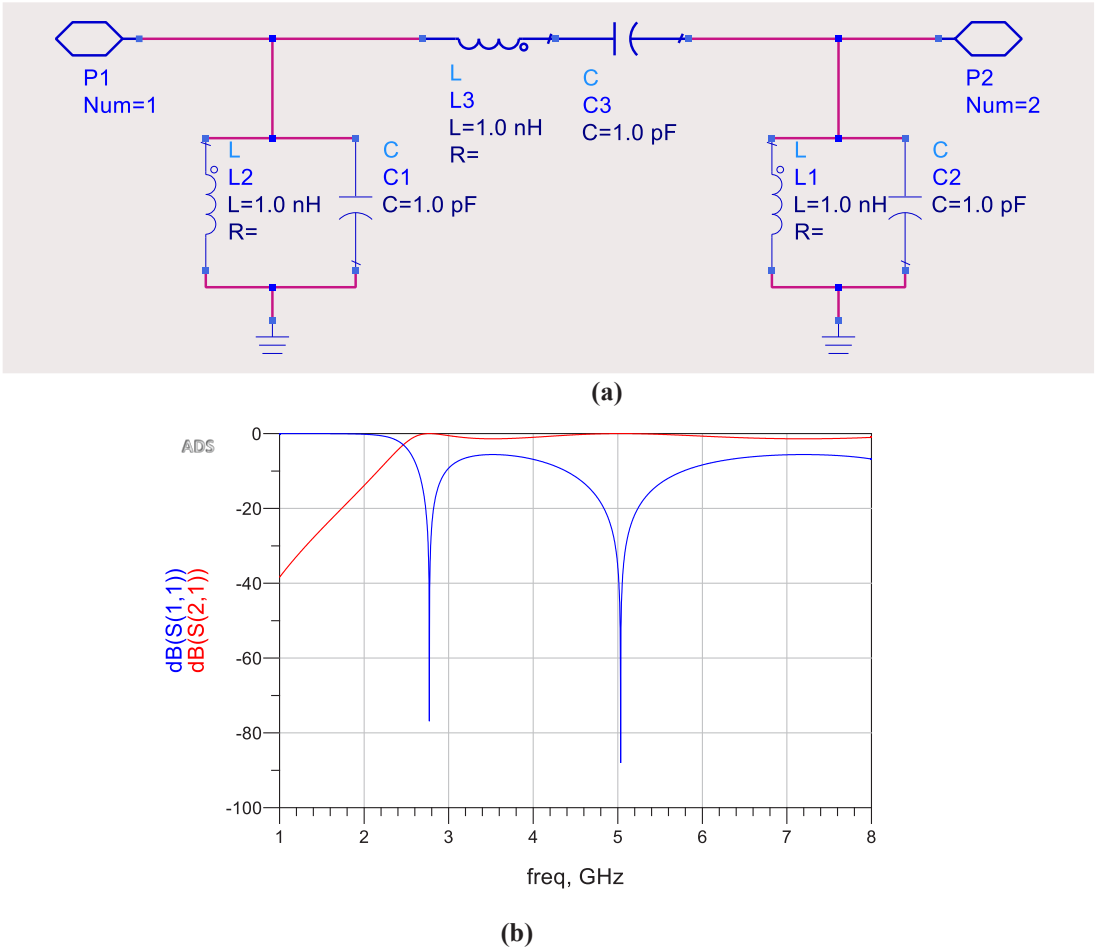


Fig. 3. a) 6th order LC bandpass filter, b) Bandpass response.

B. *The action of a band-pass filter and the use of an LC ladder*

In this section, we have presented the 6th order LC ladder filter design with all validation results. It is possible to build a band-pass filter by first synthesising a low-pass ladder circuit and then making the modifications. This process can be repeated as many times as necessary to achieve the desired results. This procedure can be carried out an unlimited number of times to attain sought-after outcomes. It is possible to use a combination that consists of an inductor and a capacitor that is also connected in series to replace inductors that are connected in series. This kind of combination would be called a series-connected combination. Both the inductor and the capacitor should each have a value that is calculated as follows: the inductor's value should be calculated as follows: Lbp = Llp / (2.BW), and the capacitor's value should be calculated as follows: Cbp = (BW.2BW) / (Llp.wo)^2. The components of the LC filter have to be selected suitably for it to be capable of achieving the desired levels of audio performance, efficiency, EMC/EMI requirements and cost for the application as a whole. Fig. 3a presents the 6th-order LC bandpass filter design and Fig. 3b present the simulation response of the LC bandpass filter design. To achieve a response that is comparable to that of the section that came before it but does not include the low pass gain, a bandpass section that is based on an LC ladder has been developed and as shown in Fig. 3a. This section was developed to achieve a response that is shown in Fig. 3b. This was done to meet the goal of creating a response that is comparable to that of the portion that came before it but does not include the low pass gain. This was accomplished by doing what was described above. Research on the s-parameter has been carried out so that it can validate that the system can be useful within the frequency range that was selected.

GM-C DESIGN

In this section, we have presented the filter Modeling, circuit implementation of Gm, biquad design using shunt LC and series LC type floating with validation results by ADS simulator. Because CMOS technology has advanced, it is now conceivable to combine analogue and digital components that are already present in the literature [20-22]. This was previously impossible. This was previously beyond the realm of possibility. It is now universally regarded as the method that has shown to be the most successful approach when it comes to the manufacturing of items in vast volumes at low prices. This is because it is the most successful technique. This is because it has been demonstrated to be the technique with the highest rate of success [20, 21]. The material known as silicon germanium is referred to by its abbreviation "SiGe." This is because RF and microwave applications have become an astounding amount more common over the previous several years. When working with radio frequency, 10 gigahertz is an important aspect to keep in mind because the CMOS technology is one of the technologies that may be utilised for a variety of applications in RF. Because of this, it is necessary to keep 10 gigahertz in mind. As a result of the efforts that have been put in to make the CMOS front end more suitable for high-frequency applications, this investigation is now within reach. Because of the efforts that have been made, the door has been opened for it, and as a result, it is now feasible to carry out this examination. It has been demonstrated that a very high level of efficiency may be achieved by combining analogue CMOS front ends with transistors and operational amplifiers. Combining these components also results in higher bandwidth. This efficiency may be quantified in terms of the amount of space that is taken up by the components as well as the amount of power that is utilised. Both of these factors are important to consider. Active forms of analogue filters are the most reliable and adaptable in terms of circuit implementation, sensitivity, and mathematical complexity; however, only a small number of analogue filters are implemented in active form. In terms of circuit implementation, sensitivity, and mathematical complexity, active variants of analogue filters have been proven to be the most reliable and versatile [23]. We may take a look at trans-conductance-capacitance (gm-C) filters as an example of the kind to get a more in-depth knowledge of this category of filter. When compared with the RC approximations of the operational amplifiers (Op-Amp), the use of CMOS gm-C filters provides consumers with several significant benefits that simply cannot be ignored. These advantages include the fact that their higher frequency ranges can be tuned simply [24], as well as the fact that gm-C and digital signal processing circuits can be fabricated on the same chip, which reduces the cost and size of the hardware while simultaneously increasing its reliability [23]. In addition, these advantages include the fact that their higher frequency ranges can be tuned simply [24]. In addition to this, one of these benefits is the ease with which their higher frequency ranges may be tuned [24]. However, there are a few downsides to employing CMOS gm-C filters: nonlinearity inherent to MOS transistors limits the acceptable signal dynamic range, and parasitic capacitances are typically substantial and must be accounted for in advance of design [26]. These drawbacks can be avoided by using a different type of filter, such as By utilising a filter of a different type, such as, for instance, Utilizing a filter of a different type, such as, for example, All of these drawbacks must be carefully considered for the best possible outcomes [18, 19, 26].

A. *Filter Modeling and Circuit design*

In this section, we have presented gyrator based inductor emulator and circuit implementation of Gm cell. To accurately reproduce an inductor, it is essential to devise a method that has been subjected to thorough testing (given below). To achieve this objective, it is required to first design a plan for, and then actually carry out, the construction of a trans-conductor that is as effective as possible (Gm). Fig. 4 is a visual representation of the Gyrator implementation concept, which is often referred to as a typical idea of inductor implementation. This concept may also be found in the context of the inductor implementation. The explanation of the idea in question is further shown by the following figures: Z_{in} is the variable that is measured and used in the process of obtaining the values of the inductive reactance for the various combinations of Gm and capacitance. As a direct consequence of this fact, it is now possible to actualize the grounded inductor in the configuration that has been demonstrated

Fig. 5 is a schematic representation of a recently reported Gm cell with dual inputs and outputs

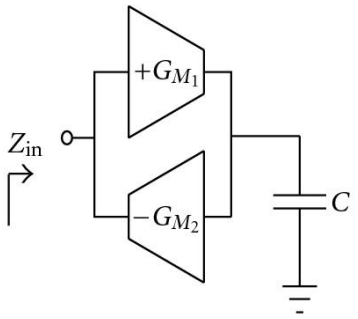


Fig. 4. Gyrator-based Inductor emulation.

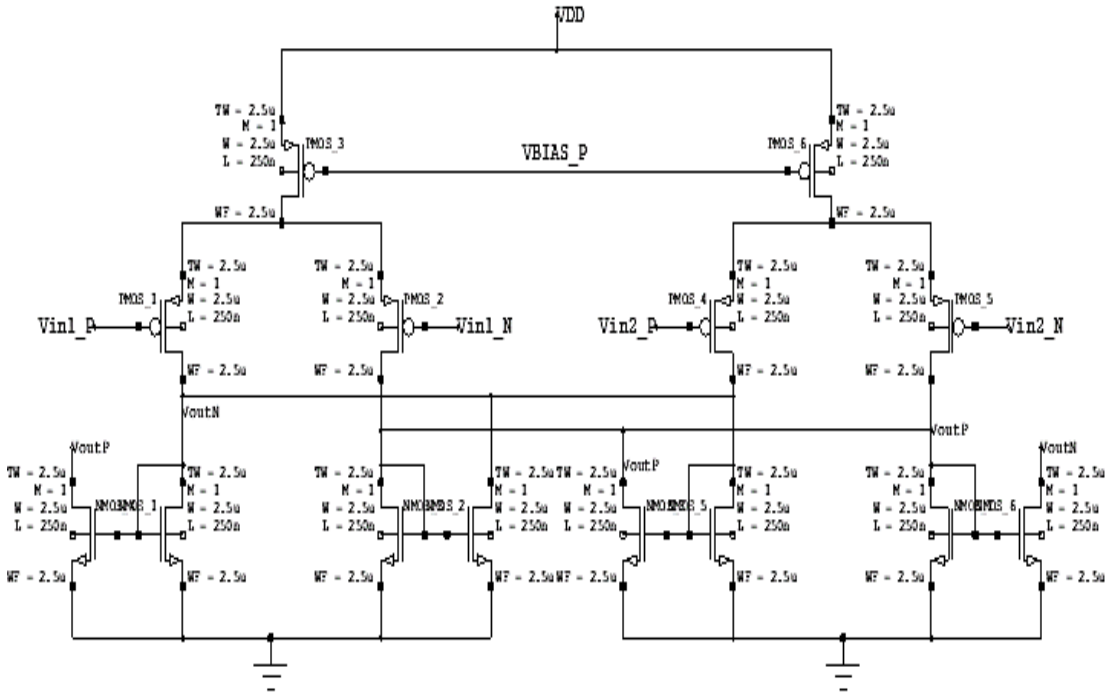


Fig. 5. Circuit implementation of proposed multi-port Gm cell.

for current sinking and sourcing capacity. This particular cell is shown because it's practical use has been demonstrated through experimentation. Numerous applications exist for this technological advancement. Low-power operation at a decent operating frequency was achieved by designing this current-mode circuit utilizing a 130 nm RF-CMOS technology. The Gm cell requires a supply voltage of 1.8 volts to operate accurately and dependably [27]. This occurs when a PMOS differential pair is used in the production of the Gm cell. Drawing has been provided only 400 microamperes of bias current.

The results of the DC analysis show that the necessary Gm for implementing the intended emulator has been obtained. This can be used to apply the full LC ladder structure after a given length of time has passed. By making the appropriate choices for the Gm and C values, the inductors that lie within the range of interest can be modelled (5 nH-100 nH).

B. *Emulating an inductor in a standard biquad section*

In this section, we have presented LC with inductor emulation and performance results. In conclusion, the Gm cell, originally developed to model an inductor, was successfully used to the simulation of a standard biquad section, commonly known as a second-order RLC structure. Second-

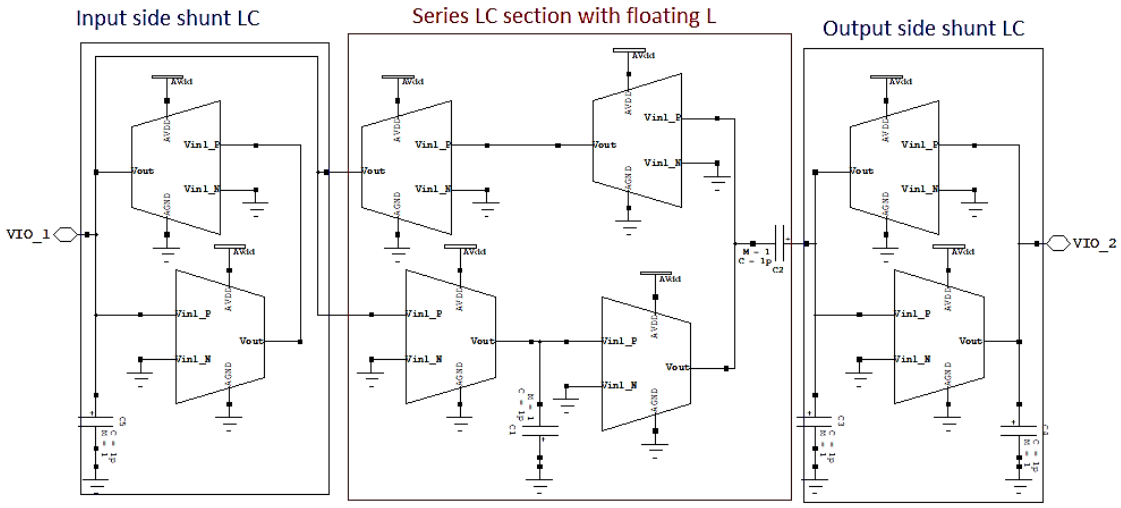
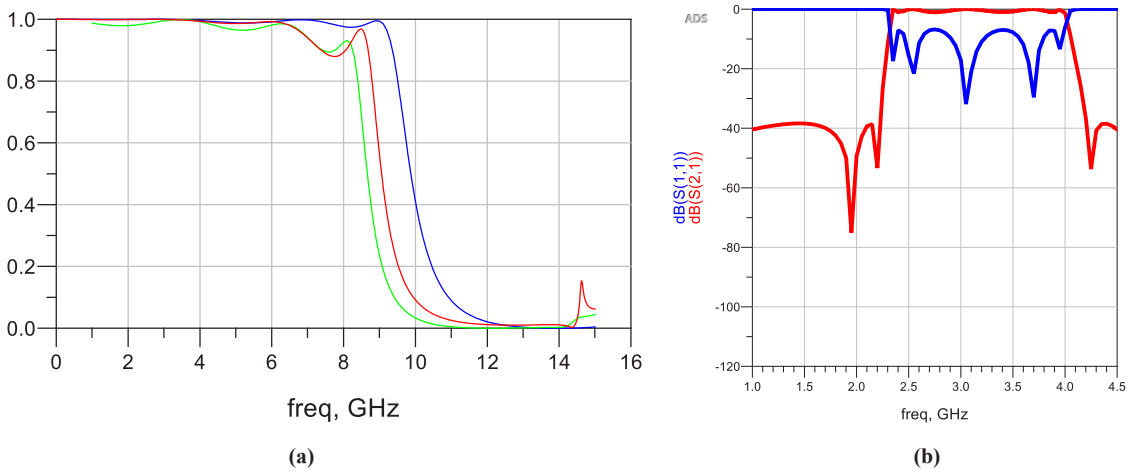


Fig. 6. LC in Fig. 3(a) implemented using inductor emulation.



(a) **(b)**

Fig. 7. (a) Low pass structure results from proposed Gm; (b) band pass structure results.

order RLC structure is another name for this type of structure. As a result, a typical biquad section might be constructed. The bandpass structure of the LC ladder is shown in Fig. 3a, which is a new addition to this study. It had been lacking from this piece up to this point. This was done to ensure that the data is not only complete, but also presented in a way that is easy to understand (Fig. 6). Two types of inductors, grounded and floating, were used in the actual implementation procedure, and the following Fig. 6 summarizes the functions of all three rungs of the ladder (see Fig. 5). Fig. 6 depicts the typical mode of operation of a single-stage differential amplifier dealing with a cross-coupled load. Applying a cross-coupled load causes the resistance to react similarly to a negative value under identical conditions. The resistance is behaving as though it was negative. One Gm cell was employed to prove the effectiveness of the offered technology in better characterizing an LPF for the purpose of this research.

The response of the bi-quad portion is presented in Fig. 7. Low pass structure results are drawn in Fig. 7a. Fig. 7b presents the bandpass structure results. It has been demonstrated that a grounded inductor simulation can be utilized to produce an effective low-pass response in the necessary frequency range (Fig. 7 (a)). As a result of this, it is possible to create tunable functioning within the frequency range of 6-8 GHz by altering the capacitance values. Because of this finding, the possibility of using changeable filters as part

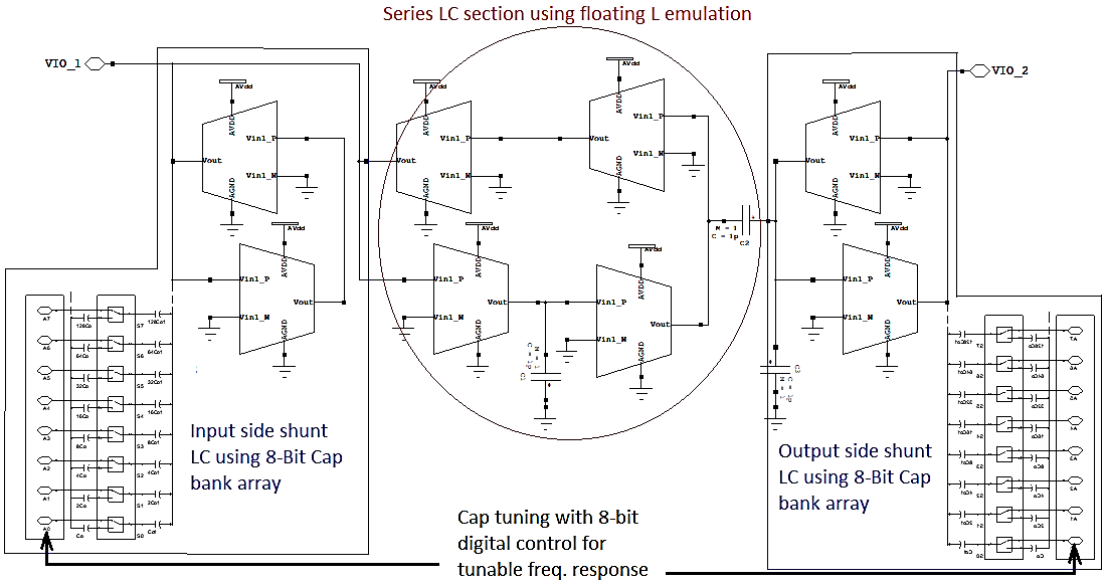


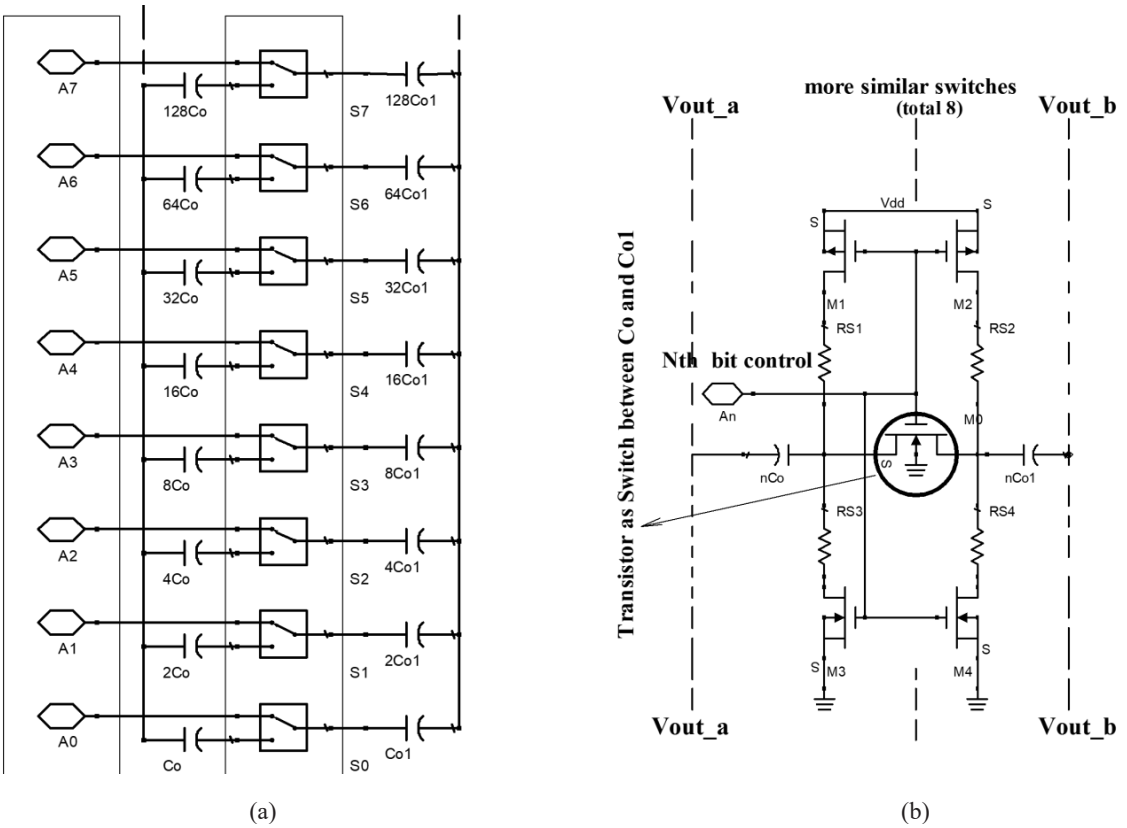
Fig. 8. Wideband Tunable filter design of Fig. 6.

of this inquiry to provide far more extensive frequency coverage is being explored.

Bandpass response data was taken from the biquad section, and this data is presented in a section of Fig. 7b. The findings are in good agreement with the targeted frequency range of 2GHz to 4GHz, and there was some additional small tuning configurability enabled by changing the values of the selected capacitors. Rather than using Gm tuning, capacitor tuning has been favoured so that a capacitor bank can cover a much wider frequency range in the next section. This has been done to make this possible. This choice was made to reduce the time for opearation. As a result of this, capacitive tuning is the one that is utilised by users the majority of the time.

IMPLEMENTATION OF A WIDEBAND, TUNABLE ORDER FILTER

In this section, we have presented wideband tunable filter, 8-Bit Cap array and performance results. In addition, the bandpass response was received from the biquad section that was implemented, and it is displayed in Fig. 7 in a manner that is distinct from the mode in which the other responses are displayed. Fig. 7(b). The values of the needed capacitors have been altered to provide a minimal degree of tuning configurability, and the results are in good accord with the anticipated frequency range of 2-4GHz. Because capacitive tuning makes it possible to cover a substantially wider bandwidth utilising a capacitor bank in the subsequent part, it was decided to make use of capacitive tuning rather than Gm tuning. This decision was made for the following reason: As a result of this, capacitive tuning was decided to be the method that would be used. To avoid the delay introduced by the switch's internal Cap-bank (in the form of parasitic delay and resistive power loss), it is preferable to utilise the external Cap-bank seen in Fig. 8 to regulate the capacitors at the input and output shunt nodes of Fig. 6. This is because the parasitic delay and resistive power dissipation that is exhibited by the switches can be reduced. This is because Fig. 8 depicts a capacitor bank that has a greater capacity than the one that is already present. This is because the switches have a degree of latency, which can be evaluated in terms of the parasitic delay and the resistive power dissipation. The time it takes for a switch to react to an input signal is known as its parasitic delay. As opposed to using analogue controls, the tuning of the Cap-DAC is accomplished externally using digital control in this particular application. Analogue controls were not used. If this hadn't been the case, then it's feasible that an 8-bit ADC would have been used instead of a continuous signal to accomplish the same goal after it was created. This would have been the case even if this hadn't been the case. The specific configuration of the Cap-DAC array is shown in Fig. 9(a), and the design of the switch



(a) (b)

Fig. 9. a) 8-Bit Cap array implementation, b) Single Cap row with Transistor switch implementation.

is depicted in Fig. 9(b). As shown in Fig. 9 (a), an increase in the total number of control bits in a filter will result in an automatic loss in gain for the filter. The primary single-cap cell is illustrated here in Fig. 9b. The frequency type voltage tunning method is used to characterise the wideband filter type, and the overlap is extremely little, coming in at approximately 10 percent of each digital bit. The wideband filter type can be distinguished from other filter types by its usage of this approach. The frequency-type voltage tunning approach is utilised to achieve this goal successfully. This strategy is utilised so that coverage may be provided for broadband frequencies. While the DAC type size is used to linearize the characteristics, the 8-bit array is utilised to cover a wider breadth while still incorporating some parasitic capacitance. Both of these methods are used in conjunction with each other. Both of these are carried out to achieve the highest possible degree of precision in the measurements.

Using the cap-bank illustrated in Fig. 8 to manage the capacitors at the input and output shunt nodes of Fig. 6 is preferable to using the cap-bank contained within the switch, which introduces latency in the form of parasitic delay and resistive power dissipation. For one, Cap-bank switches introduce some delay due to parasitic delay and resistive power dissipation. The switches' potential to reduce parasitic delay and resistive power dissipation makes this a real possibility. Since a cap-bank is shown in Fig. 8, that's the reason for this particular case. Fig. 6 depicts a cap-bank. This is because the switches experience a certain degree of latency as a result of the parasitic delay and the resistive power loss. This causes the switches to have a certain level of delay. The fact that the switches have a certain amount of latency is the cause for this behaviour. Utilizing digital control allows the tuning of the Cap-DAC to be carried out in a different position from where it was originally located in this specific application. Utilization of the internet paves the way for the realisation of this possibility. If this had n't been the case, an 8-bit ADC would have likely relied on a continuous signal to accomplish the same task. It's possible that this wouldn't have happened if this hadn't happened. Fig. 9a

Table 2. Design parameters.

Parameters	Results	
L= 1 nH	f_{min}= 2.4 GHz (for V_{bit}, max= 11111111)	f_{max}= 5.4 GHz (for V_{bit}, min= 00000000)
Required C_{total} = C_{var} + $C_{capbank}$	C_{total} (max) = 4400 fF	C_{total} (min) = 700 fF
MOS sizing (W/L) 200 μm/0.48 μm	227 fF for V_{tune}= 1.2 V (max) 247 fF for V_{tune}= 0 V (min)	
Maximum $C_{capbank}$ required (for f_{min} corresponding to V_{bit}=11111111)	4000 fF	

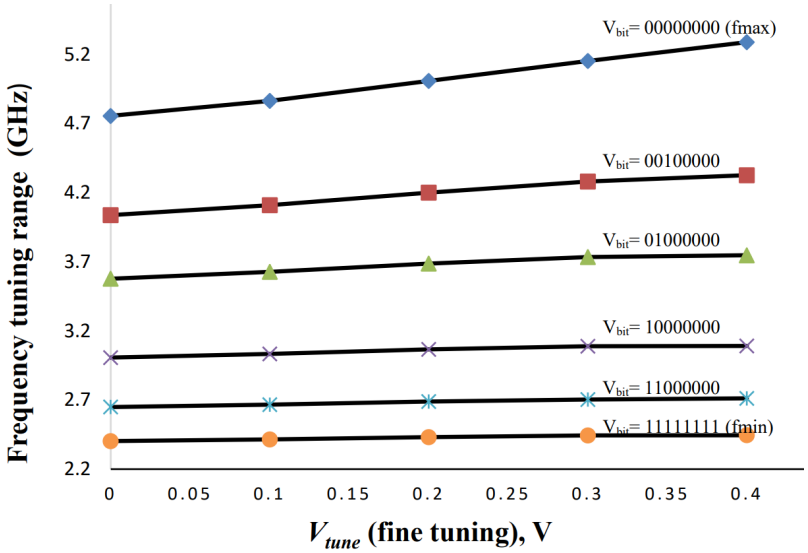


Fig. 10. Frequency coverage by Cap-bank array using 8-bit control.

depicts the overall layout of the Cap-DAC array, and Fig. 9b shows the design of the switches. We, can access both of these diagrams via the links provided further down the page. For any given filter, increasing the amount of control bits will result in a lower gain (Fig. 9 (a)). Because the gain scales with the number of control bits, this is the case. Fig. 9 depicts a single subcellular component of this overall cellular architecture (b). Overlap is extremely small, equivalent to roughly ten percent of each digital bit, and is used to characterise the wideband filter type via the frequency type voltage tunning method. To classify the variety of wideband filters, the frequency type voltage tunning technique is applied. Using the frequency-type voltage-tuning method, one can attempt to classify the wideband filter design in use. Using this method, you can ensure protection for wide-band frequencies. The 8-bit array is utilised to cover a wider breadth while still incorporating some parasitic capacitance, and the DAC type size is employed to linearize the characteristics. In clinical settings, it is common to use both of these approaches simultaneously. When seeking optimal outcomes, clinicians often blend these two methods. Table 2 presents the design parameters with all details.

The frequency coverage that will be offered by the proposed cap-bank array was simulated making use of a testbench, and the outcomes are displayed in Fig. 10. This estimation receives support from the findings of the simulation, which are going to be discussed in the next sections of the document. Because these data demonstrate

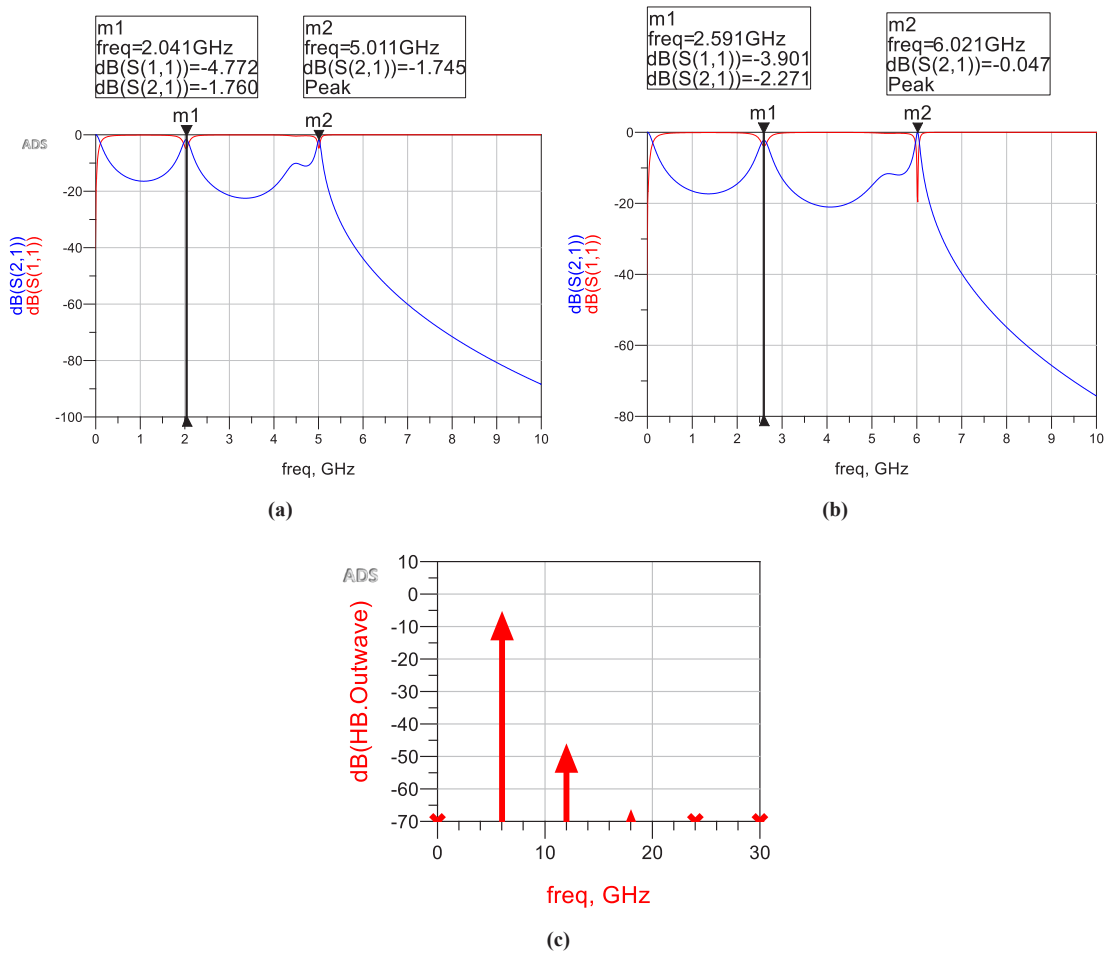


Fig. 11. a) Frequency of the tunable filter, b) highest control signal and, c) Output signal.

that the Cap-bank plays a significant role in the ability of the filter to be altered, we can conclude that this estimate is accurate. The Cap-bank is what enables the tunability component of the suggested LC filter design (which was mentioned in the previous chapter), which is carried out with the help of GmC-based emulators and then put into action in the following section. The section that came before it provides support for this component. The section that came before it offers support for the component that is being discussed here. The component's steadiness is tied to the stability of the part that came before it in the assembly process. This cap-bank structure, which was simulated for the s-parameters to ensure that they are accurate, serves as the basis for the wideband tunable filter that is shown in Fig. 8. This filter can be customised to accommodate a wide range of frequencies. The frequency coverage that will be offered by the proposed cap-bank array was simulated by making use of a test bench, and the outcomes are displayed in Fig. 10. This estimation receives support from the findings of the simulation, which are going to be discussed in the next sections of the document. As a result of these data, which demonstrate that the Cap-bank plays a vital part in the ability of the filter to be modified, we can conclude that this estimate is accurate. The Cap-bank is what enables the tunability component of the suggested LC filter design (which was mentioned in the previous chapter), which is carried out with the help of GmC-based emulators and then put into action in the following section. The section that came before it provides support for this component. The component that it is based on receives assistance from the section that came before it. The component's steadiness is tied to the stability of the part that came before it in the assembly process. The wideband tunable filter depicted

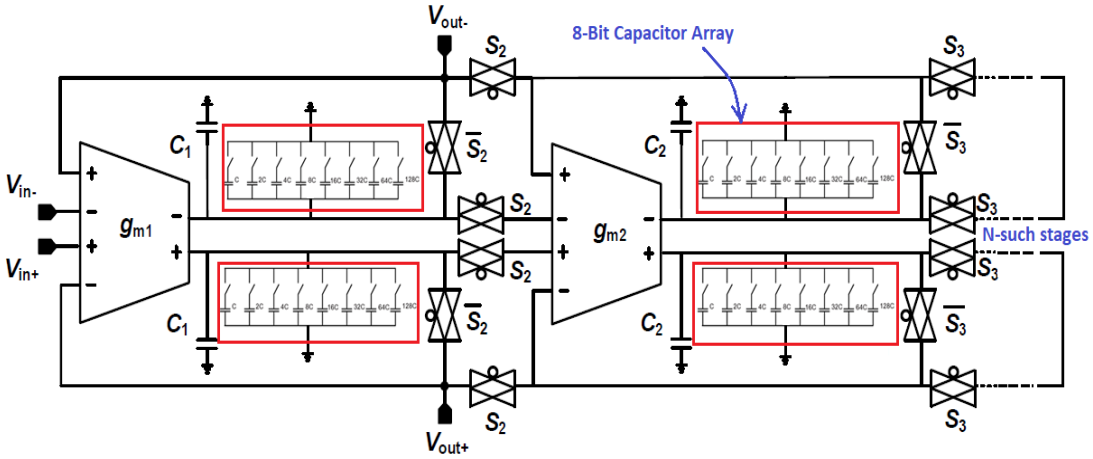


Fig. 12. Proposed reconfigurable MLF low pass structure.

in Fig. 8 is based on this cap-bank structure, the s-parameters of which were simulated to guarantee accuracy.

Fig. 11 displays the outcomes of a wideband tuning operation performed on the bandpass filter's design. These results are an indirect result of putting the method into practice. Fig. 11(a) and (b) depict the bands with the least frequency coverage (for Vbit = 11111111 of Cap-bank) and the bands with the most frequency coverage (for Vbit = 00000000 of Cap-bank), respectively (2.4 GHz and 5.4 GHz). All evaluated quality factors (QFs) for both the 2.4GHz and 5.4GHz bands landed in the 27–39 range. This held irrespective of the group they supported. In Fig. 11c, we see a visual representation of the filtered output quality at 6 GHz after implementing a switchable filter. This corresponds to the maximum setting that may be achieved within the tuning range, which can be seen in Fig. 11(b). The noticeable second harmonic, which can be interpreted as a noise component in Fig. 11(c), is the result of a poor quality factor, which is ultimately a consequence of targeting tunable bandwidth from a single filter structure. In other words, the second harmonic is a result of a poor quality factor. To put it another way, the appreciable second harmonic is the consequence of a quality component that is subpar. To put it another way, the presence of a discernible second harmonic is the direct result of a quality component that is below standard. In addition to the ON and OFF resistances that are provided by those switches, the switches that are integrated into the capacitor bank also supply the dynamic resistance. This resistance is provided by the switches. As a direct consequence of this element, the filter's performance in terms of its selectivity will ultimately be enhanced. Fig. 9 is the best example that can be found to illustrate this argument (b). This harmonic content is positioned forty decibels below the fundamental, and it provides the same level of noise performance that the fundamental does. Table 3 provides a summary of the quality of the filtered signal in this particular instance, which demonstrates why some modifications to the selectivity of the filter are necessary. Table 3 presents the input frequency versus harmonic content.

In addition to the wideband operation of the filter, it is possible to experiment with a switchable order structure; the concept is depicted in the Fig. 12. It might be possible to build high-frequency transmission gates and switches, which, if implemented, would allow the order of the filter structure to be reconfigured across some N-number of stages.

A filter with a movable order structure as shoen in Fig. 12 is applicable for wideband application. It is possible to build high-frequency transmission gates and switches, which would make it possible to reconfigure the order of the filter structure's stages using some N-number of them.

Table 4 compares the performance of a low-power tunable filter to that of previous works. The performance of switchable filters at different process corners was simulated by measuring their responses in voltage, current, trans-resistance, and transconductance modes. All of the aforementioned modes are simulated with the proposed filter, and supply voltages are

Table 3. The input was filtered, and the output had harmonic content centered at about 6 GHz.

Freq	HB Vdrain
0.0000 Hz	2.820 / 0.000
6.000 GHz	0.446 / 100.608
12.00 GHz	0.004 / 42.036
18.00 GHz	3.874E-4 / 158....
24.00 GHz	1.722E-4 / -97....
30.00 GHz	9.041E-5 / 6.288

Table 4. Performance comparison of the proposed Low power tunable filter with other published works.

Specifications	Ref [11]	Ref [18]	Ref [21]	Ref [28]	Ref [29]	This work
Technology	0.18 μm	0.8 μm	0.13 μm	0.13 μm	65-nm	0.13 μm *RF-CMOS*
V_{dd} (Supply), *V*	1.2	3.5	1.2	1.2	1.2	1.2
Frequency Coverage (f_o or Δf)	500 KHz- 20 MHz	100 MHz	5.4–5.495 GHz	4.3-5.2 *GHz*	Δf =50 MHz	2 GHz- 6 *GHz*
Filter order	3	4	-	-	14.12	7 (LPF), 6 (BPF)
Noise Performance	Input referred Noise density of 128-425nV/$\sqrt{Hz}$	PN of -65 dBc/Hz at 100kHz offset	PN of -160 dBc/Hz at 1 MHz offset	PN of -164 dBc/Hz at 1 MHz offset	Input referred Noise density of 5nV/$\sqrt{Hz}$	PN of -40 dBc/Hz at 1 MHz offset
Power Dissipation (mW)	4.1 - 11.1	-	6.52	12	19.8	4.3

varied about the nominal value by a factor that is 10% greater than the standard deviation. In this way, the effect of varying voltages on the filter parameters can be investigated in more depth. The filter's centre frequency was not expected to be affected by the voltage change and would therefore stay unaffected. After introducing our low pass and bandpass LC ladder filter, we'll go through how well it performs in general. The GmC was used in a configuration that enabled broad-band. There are also several comparisons between the current designs and state-of-art-works. Incorporating the described GmC-based LC ladder filter into the analogue front end of already-in-wireless systems is expected to maximize their usability. This is the tunable filter in terms of the very desired properties of low power consumption and wideband tuning.

CONCLUSION

Transconductance-based current-mode LC-ladder filters have been created systematically employing 130nm-RF CMOS technology. The inclusion of a wideband tuning element was considered throughout development. In order to show high-frequency operation in a form that can be modelled using s-parameters, we are developing working prototypes of both a seventh-order low pass filter and a sixth-order band pass filter. This design intends to show high-frequency operating in a way that is relatively accessible to s-parameter modelling. We will do this by combining both types of filters. During the low pass and band pass realisations, all inductive components are grounded while the rest of the components are left to float. This is done to enable both the low pass and band pass realisations to take place. Particularly useful is the GmC-based Gyrator, which also helped with the low-power current mode aspect of the equation. Using an array of 8-bit capacitors, the user can generate a cut-off frequency that can be fine-tuned based on the chosen parameters. Before making any changes to the grounded sensitive nodes of the filter, this step must be done by changing the Gm and capacitance amounts of the cap-bank,

the intended wide behaviour in the current wireless band could be achieved. As a result, the maximum level of performance is feasible (2GHz-6GHz). To evaluate the frequency response and noise performance of the proposed structure, simultaneous SPICE and RF (s-parameter, harmonic balancer) simulations were performed in ADS. When compared to existing work, the proposed Low power tuneable filter stands out due to its enhanced different parameters.

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CONFLICTS OF INTEREST

The authors do not have any conflicts of interest.

AVAILABILITY OF DATA AND MATERIAL

Not Applicable.

CODE AVAILABILITY

Not Applicable.

COMPLIANCE WITH ETHICAL STANDARDS:

The authors declare that they have no known competing financial interests or

personal relationships that could have appeared to influence the work reported in this paper.

CONSENT TO PARTICIPATE

Not applicable.

CONSENT FOR PUBLICATION

Not applicable as the manuscript does not contain any data from individual.

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