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ORIGINAL ARTICLE

A fast approximate quaternary full adder using a parallel design based on Carbon Nanotube FET

Alireza Bolourforoush[1], Mokhtar Mohammadi Ghanatghestani[2,]*

[1] *Department of Computer Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran*
[2] *Department of Computer Engineering, Bam Branch, Islamic Azad University, Bam, Iran*

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Abstract
Novel design methodologies of digital circuits have been caught in the spotlight of attention as a result of the dramatic increase in available data and the requirement for data processing among which Full adder cells are significant elements in arithmetic circuits design. The use of approximate computing and Multi Value Logic (MVL) can improve computational circuit efficiency. Carbon Nano Tube Field Effect Transistors (CNTFETs) with an adjustable threshold voltage is effective in the design of MVL circuits. This paper proposes a new CNTFET-based approximate quaternary full adder to reduce the area, delay, and power consumption. The Synopsys HSPICE results obtained based on 32nm Stanford CNTFET technology showed that the proposed model had much lower average power consumption, delay, power-delay product (PDP), and size as compared to other approximate full adders.

Keywords: *Approximate Computing; Critical Path delay; Full Adder Cell; Multi Value Logic; Quaternary logic.*

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INTRODUCTION

The wide use of graphic processors has made highlights the importance of low-power circuit design. Moreover, miniaturization of Metal Oxide Semiconductor Field Effect Transistors (MOSFET s) faces encountered challenges such as short channel effect, high leakage power, damaged gate control, parametric variation, and higher power densities [1]. The frequency enhancement of processors somewhat meets processing demands in the current applications; however, it also increases power consumption in the circuit [2]. The reduction of the power supply voltage and switching frequency can reduce power consumption. However, such techniques have disadvantages, e.g., increased leakage currents and parasite capacitances [3]. Due to the CNTFET and MOSFET intrinsic similarities and P- and N- transistors existence, CNTFET could be an efficient alternative to MOSFET. CNTFETs could be more efficient in the design of MVL circuits as their threshold voltage can be adjusted by setting the CNT diameter which makes. [4]. The equal excitation of P- and N-type transistors and threshold voltage adjustment through CNT size tuning are other advantages of CNTFETs [5]. Multiplicity of internal connections remains a major challenge of binary integrated circuits. To deal with such challenges, MVL can be adopted rather than binary logic. Many logical and mathematical operations can be performed in fewer steps using MVL [6]. Besides MVL reduces chip complexity and surface area. Quaternary logic can be employed in place of binary logic to represent a number with fewer bits [7].

Computational complexity is often a major characteristic of signal processing algorithms, and therefore the circuit switching speed can become an advantage [8]. To improve circuit parameters such as power consumption, delay, and size, approximate computing has been a satisfactory approach. Circuits could handle hardware limitations through significant accuracy

* Corresponding Author Email: *mokhtarmohamadi@srbiau.ac.ir Tel.: +989132989005*

[9]. Approximate computing in computational circuits is an emerging technique to reduce power consumption and transistors. In other words, approximate computing is a new method to decrease power consumption and circuit size and consequently parasite capacitances and leakage currents. In contradiction, it reduces circuit accuracy proportionally [9,10]. Furthermore, the shortening of critical paths enhances the performance and speed of the circuit, decreases the supply voltage, and reduces manufacturing costs [11]. Approximate computing would substantially improve the performance of specific processors, such as digital signal processors [12]. In general, approximate computing is a promising technique in fault-tolerant applications. Fault tolerant applications are those in which the difference between the exact and approximate outcomes is not easily detectable to humans, such as image processing [13]. Approximate computing is applied to implement data processing in cases such as machine vision, data mining, pattern recognition, and signal processing, etc. Images and videos account for a major portion of the common multimedia applications for representation and human analysis. Hence, approximate computing could be effectively used in such applications [14]. Full adders have become a crucial component of arithmetic circuits as they are employed in series and parallel n-bit adders, subtractors, multipliers, and other computational circuits. Furthermore, full adders are used in Field Programmable Gate Arrays (FPGAs). Therefore it is necessary to design full adders of high performance and low power consumption [15]. Full adder cells are a major block of circuits, and their improvement substantially improves other larger blocks.

Therefore, a new Approximate Quaternary Full Adder (AQFA) with a parallel structure was proposed using multiplexers. In addition, it was implemented based on a combination of Transmission Gates (TGs) and pass Transistor Logic (PTL). As a result, the output of the circuit would enable full swing. As mentioned, the attitude toward technology, logic design and computational techniques has been changed in order to achieve energy or power consumption efficiency in full adders. This study adopted CNTFET technology, quaternary logic, and approximate computing. The proposed cell was compared to other full adders, demonstrating the power consumption, delay, and Power-Delay Product (PDP) as the advantages of the proposed full adder. The remainder of the paper is organized as follows: reviews the CNTFET literature; explains the quaternary logic; reviews the full adders that would be compared to the proposed model; describes the proposed QFAs; provides the numerical results and compares the proposed model to other systems; and concludes the work.

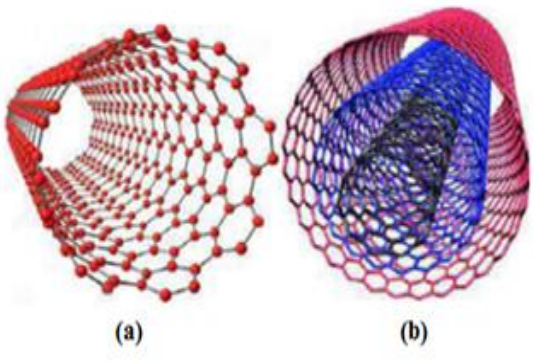

Fig. 1. 3D structure of carbon nanotubes (a) single-walled and (b) multi-walled CNTs [19].

Nano-scaled MOSFETs with a size of 65 nm were introduced in 2006 [16]. Silicon MOSFETs had major drawbacks, such as parametric variation and increased leakage current. Then, alternative technologies, e.g., CNFETs, were introduced to handle drawbacks of nano-scaled MOSFETs [17]. Nanotubes between the source and drain are the main structural difference between CNFETs and MOSFETs. These nanotubes arise from the rotation of a graphene plate around a certain axis [18]. Nanotubes are architecturally divided into Single Walled Nano Tubes (SWNTs) and Multi Walled Nano Tubes (MWNTs) which are shown in 3D in Fig. 1a, and Fig. 1b, respectively. SWNTs are further classified based on the carbon atom arrangement of the tube section into armchair, chiral (metallic properties) and zigzag (semiconducting properties) groups [19]. An SWNT can appear in the form of a graphite plate (hexagonal carbon lattice) curved into a cylinder with a Nano-scaled diameter and a micro-scaled length [20].

Each geometric structure can be defined by its peripheral vector with two constituent integers n_1 and n_2. Typically, graphite plates are considered as simple and unrolled plates. Then, the rolling process is represented by vectors $\vec{a}_1$ and $\vec{a}_2$ and the vector formulated in Eq. (1), where n_1 and n_2 are integers [21].

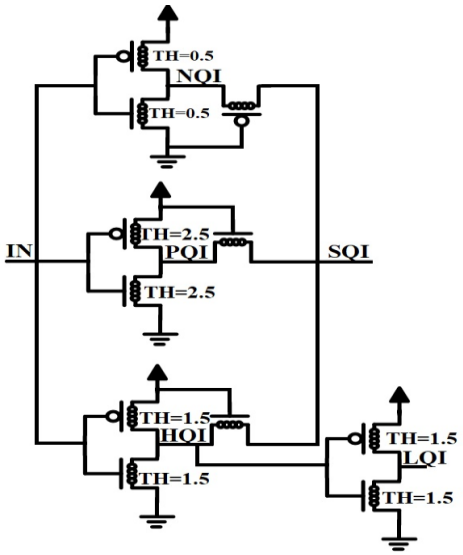

Fig. 2. The circuit of inverters used in the proposed design.

$$\vec{R} = n_1.\vec{a}_1 + n_2.\vec{a}_2 \quad (1)$$

Nanotubes can be changed from metallic or semi-metallic into semiconductors by altering n_1 and n_2. Nanotubes are metallic for $n_1 = n_2$, semi-metallic for $n_1 - n_2 = 3j$, where j is a non-zero integer, and semi-conductor for $n_1 - n_2 = 3j \pm 1$, where j is an integer. Here, the CNT circumference C_h is calculated by Eq. (2)

$$C_h = a\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (2)$$

where a is the difference between two C atoms (2.4 nm). The diameter of the nanotube is calculated by Eq. (3).

$$D_{CNT} = C_h / \pi \quad (3)$$

The threshold voltage is the voltage required to switch on CNTFETs. The threshold voltage of CNT channels is inversely related to the CNT diameter, which is approximated in Eq. (4). Here, $V_\pi = 3.033\ eV$, and e is the unit electron charge. Furthermore, D_{CNT} denotes the CNT diameter. The CNTFET threshold voltage changes once the chirality vector changes. This is exploited in the design of MVL circuits [21, 22].

$$V_{th} = \frac{Eg}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \quad (4)$$

Three types of CNFETs have been developed. Schottky Barrier CNFETs (SB-CNFETs) are designed based on metal-nanotube, semiconductor-metal connections. They operate based on direct tunnelling through the Schottky barrier that arises from undesirable connections between the metal and semiconductor.

SB-CNFETs deliver a low on-current. Thus, they do not suit applications with high performance requirements. Band-to-band Tunnel CNFETs (T-CNFETs) have low on-current and excellent cut-off. Therefore, T-CNFETs are effective for low-power applications. MOSFET-like CNFETs show field-effect and unipolar behaviour. In contrast to SB-CNFETs and T-CNFETs, MOSFET-like CNFETs do not show SB effects since the same source-channel and channel-drain connection materials are employed. MOSFET-like CNFETs have high on-current and suit high-performance applications [23, 24]. This study used MOSFET-like CNFETs in the design of the proposed approximate QFA cells.

Binary logic uses only 0 and 1 to represent data. The processing, storage, and transmission of large amounts of data in digital signal processing are major challenges of binary systems. MVL can be employed as an alternative to handle such challenges. The advantages of MVL currents include faster computations, higher storage densities, and fewer pins and internal connections in integrated circuits for efficient low-power design applications [25].

Quaternary logic is implemented using four logic values of 0, 1, 2, and 3, represented by voltages of 0, vdd/3, 2vdd/3, and vdd. To develop a quaternary inverter, SQI, PQI, NQI, HQI, and LQI models were considered. Actually LQI is the inverse of HQI output. Table 1 reports these models using logic values of 0, 1, 2, and 3. The proposed inverter circuit is shown in Fig. 2. This inverter is designed in such a way that the output of all five inverters includes negative (NQI), positive (PQI), high level (HQI), low level (LQI) and standard (SQI).

Adders are the main computing unit in digital signal processors. Adder circuits are a major component of arithmetic circuits. The performance of an adder determines performance of the system to a great extent and this is evidence

Table 1. Truth table of the quaternary inverter.

Input Variable	SQI	PQI	NQI	HQI	LQI
0	3	3	3	3	0
1	2	3	0	3	0
2	1	3	0	0	3
3	0	0	0	0	3

Table 2. Truth table of a QFA cell.

$\sum \text{in} = A_i + B_i + Cin$	Cout	Sum
0	0	0
1	0	1
2	0	2
3	0	3
4	1	0
5	1	1
6	1	2
7	1	3
8	2	0
9	2	1

of the importance of the design and enhancement of adder circuits. A full adder cell has three inputs and two outputs, and the outputs are the sum of inputs. Here, A_i and B_i are digits *i* of numbers A and B, respectively, and input C_{in} is obtained from the previous adders and is the other input of the quaternary adder cell. Table 2 shows the truth table of a QFA cell [26].

Two optimized quaternary half adders (QHAs) and a quaternary carry generation unit were proposed [29]. The system effectively used PTL to reduce the number of transistors. The PTL design was adopted to induce cascading in QFA to generate larger adders, e.g., QRCA. As a result, the output signal of each QFA does not affect the QFA transistor drain of the next level. A quaternary decoding (QDEC) circuit was also used in the QFA cell. Two inverters were employed to obtain the required inputs of the QHA.

The inputs of the inverters were the output of the QDEC. In [30] a new design of quaternary multiplexer 4:1 with carbon nanotube field-effect transistors (CNFETs) is proposed. Afterward, quaternary successor, quaternary predecessor, and quaternary second-level successor cells are, for the first time, introduced based on CNTFETs. They reduced the number of transistors by using three power supplies. Previous studies aimed to shorten the critical path in a QFA circuit using a parallel design with positive effects on the speed and power consumption [30]. The circuit had unique characteristics, such as a satisfactory threshold voltage by altering the nanotube diameter in the transistors. In [26], a formulation was developed for each output, and a quaternary multiplexer was employed to implement the internal components of the final circuit.

MATERIALS AND METHODS

The proposed QFA cell is described here. PTL may diminish the number of transistors, area, and power consumption within integrated circuits. AQFAs are intended to be optimized in terms of delay, power consumption, and area. Fig. 3. illustrates the implementation of an AQFA, consisting of quaternary inverters, carry generation components ($Cout_{+i}$) and sums (Sum_{+i}), and a QHA. The QHA was designed and implemented in [31].

As shown in Fig. 3, the circuits Sum_{+1}, Sum_{+2}, and Sum_{+3} are dependent only on Sum_0 obtained from the QHA, and the output of each level is independent of those at the previous and next levels. Table 3 represents the truth table to capture the relationship between Sum_{+i} and $Cout_{+i}$. It contains A, B, and C_{in}. Here, C_{in} could be set to 0, 1, 2, or 3, and the carry adder output represents the exact and approximate sums.

The approximations assumed for Cout generators had a difference of only one unit from the real value. The proposed design does not implement changes to obtain Sum_{+i} and provides the exact value. However, the $Cout_{+i}$ of the AQFA is essentially altered to shorten the critical path.

The proposed circuit has fewer transistors than other circuits. N-type transistors are good transmitters for zero voltage, and P-type transistors are good transmitters for Vdd voltage. In the proposed design, the zero voltage flows through the N-type transistors, while Vdd flows through the P-type transistor, with Vdd/2 and Vdd/3 flowing through a parallel combination of N- and P-type transistors. Each transistor with a suitable TH determines whether the transistor is on or off. The TH is a threshold of 0, 1, 2, or 3 to represent 0.5, 1.5, and 2.5, respectively. The TH of no-input transistors is normal; however, the other N- and P-type threshold voltages ($V_{th,\,n}$ and $V_{th,\,p}$) are given by Eq. (11) & Eq. (12).

$$\text{Vth, n} = \frac{\text{TH} * \text{Vdd}}{4} \tag{11}$$

$$|\, V_{th,p} \,| = V_{dd} - V_{th,n} \tag{12}$$

N-type transistors are switched on when their gate input receives a voltage above $V_{th,n}$. This voltage level switches off the P-type transistors [32].

Fig. 3 (a). shows the sum_{+1} circuit. In this circuit, the threshold voltage of transistors, T2, T4, T5, T7 are normal, while the threshold voltage of the rest of the available transistors represents the generation of desired output. The threshold

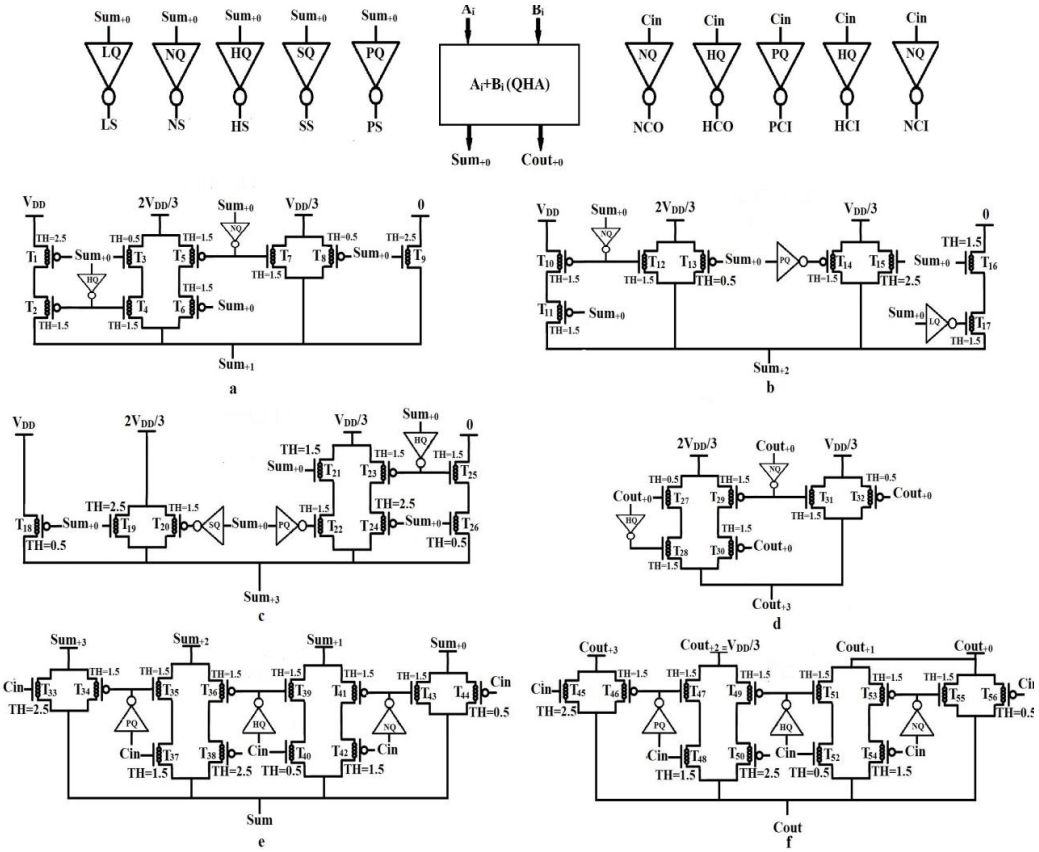

Fig. 3. Proposed Approximate Quaternary Full Adder cell (a) Sum_{+1} (b) Sum_{+2} (c) Sum_{+3} (d) $Cout_{+3}$ (e) Sum (f) Cout.

Table 3. Truth table of the proposed AQFA.

A	B	Cin=0		Cin=1			Cin=2			Cin=3		
		Sum_{+0}	Exact $Cout_{+0}$	Sum_{+1}	Exact $Cout_{+1}$	Approximate $Cout_{+1}$	Sum_{+2}	Exact $Cout_{+2}$	Approximate $Cout_{+2}$	Sum_{+3}	Exact $Cout_{+3}$	Approximate $Cout_{+3}$
0	0	0	0	1	0	0	2	0	1×	0	0	1×
0	1	1	0	2	0	0	3	0	1×	1	1	1
0	2	2	0	3	0	0	0	1	1	1	1	1
0	3	3	0	0	1	0×	1	1	1	1	1	1
1	0	1	0	2	0	0	3	0	1×	1	1	1
1	1	2	0	3	0	0	0	1	1	1	1	1
1	2	3	0	0	1	0×	1	1	1	1	1	1
1	3	0	1	1	1	1	2	1	1	1	1	2×
2	0	2	0	3	0	0	0	1	1	1	1	1
2	1	3	0	0	1	0×	1	1	1	1	1	1
2	2	0	1	1	1	1	2	1	1	1	1	2×
2	3	1	1	2	1	1	3	1	1	2	2	2
3	0	3	0	0	1	0×	1	1	1	1	1	1
3	1	0	1	1	1	1	2	1	1	1	1	2×
3	2	1	1	2	1	1	3	1	1	2	2	2
3	3	2	1	3	1	1	0	2	1×	2	2	2

voltage value of transistor T9 is determined in order that the logic value of input Sum_{+0} is only equal to three. The threshold voltage value of transistor T8 is determined in a way that the logic value of input Sum_{+0} is considered equal to zero. The threshold voltage value of transistor T6 is determined in order that the logic values of input Sum_{+0} can be considered zero or one. The threshold voltage value of transistor T3 is determined in a way that the logic values of Sum_{+0} can be considered one, two, or three, and finally the threshold voltage value of transistor T1 is determined in order that the logic values of input Sum_{+0} can be zero, one or two. Sum_{+1} circuit is obtained from Eq. (5).

$$\mathrm{Sum}_{+1}=\begin{cases}1 & \text{if } \mathrm{Sum}_{+0}=0\\ 2 & \text{if } \mathrm{Sum}_{+0}=1\\ 3 & \text{if } \mathrm{Sum}_{+0}=2\\ 0 & \text{if } \mathrm{Sum}_{+0}=3\end{cases} \quad (5)$$

Fig. 3(b). shows the sum_{+2} circuit. The threshold voltage of the transistors T10, T12, T14, T17, is normal, while the threshold voltage of the rest of the available transistors is such that the desired output is generated. The threshold voltage value of transistor T16 is determined in order that the logic values of input Sum_{+0} can be considered equal to two or three. The threshold voltage value of transistor T15 is determined in a way that the logic value of input Sum_{+0} is only equal to three. The threshold voltage value of transistor T13 is determined in order that the logic value of input Sum_{+0} is considered to be zero. The threshold voltage value of transistor T11 is determined in a way that the input values of Sum_{+0} can be zero or one. Sum_{+2} circuit is obtained from Eq. (6).

$$\mathrm{Sum}_{+2}=\begin{cases}2 & \text{if } \mathrm{Sum}_{+0}=0\\ 3 & \text{if } \mathrm{Sum}_{+0}=1\\ 0 & \text{if } \mathrm{Sum}_{+0}=2\\ 1 & \text{if } \mathrm{Sum}_{+0}=3\end{cases} \quad (6)$$

Fig. 3(c). shows the sum_{+3} circuit. The threshold voltage of the transistors T20, T22, T23, T25, is normal, while the threshold voltage of the other transistors is such that the desired output is generated. The threshold voltage value of transistor T26 is determined in order that the logic value of input Sum_{+0} is considered to be one, two or three. The threshold voltage value of transistor T24 is determined in a way that the logic values of input Sum_{+0} can be considered as zero, one or two. The threshold voltage value of transistor T21 is determined in order that the logic values of input Sum_{+0} can be considered equal to two or three. The threshold voltage value of transistor T19 is determined in a way that the logic value of the input Sum_{+0} is considered to be only three, and finally the threshold voltage value of transistor T18 is determined in order that the logic value of input Sum_{+0} can only be considered zero. Sum_{+3} circuit is obtained from Eq. (7).

$$\mathrm{Sum}_{+3}=\begin{cases}3 & \text{if } \mathrm{Sum}_{+0}=0\\ 0 & \text{if } \mathrm{Sum}_{+0}=1\\ 1 & \text{if } \mathrm{Sum}_{+0}=2\\ 2 & \text{if } \mathrm{Sum}_{+0}=3\end{cases} \quad (7)$$

In Table 3, the check sign × denotes inexact values. Once Cin is 1 and (A, B) inputs are (0, 3), (1, 2), (2, 1), and (3, 0), C_{out+1} is assumed to be 0. Thus, $Cout_{+1}$ is written as Eq. (8).

$$Cout_{+1}=Cout_{+0} \quad (8)$$

For C_{in}=2 and (A, B)=(0, 0), (0, 1), (1, 0) and (3, 3), the approximate $Cout_{+2}$ is assumed to be 1 or ($V_{dd/3}$) and $Cout_{+2}$ is given by Eq. (9).

$$Cout_{+2}=1 \quad (9)$$

For C_{in}=3 and (A, B)=(0, 0), approximateC_{out+3} is 1.

Furthermore, for (B, A)=(1, 3), (2, 2), and (3, 1), approximate C_{out+3} is assumed to be 2. Then, C_{out+3} is given by Eq. (10).

$$\mathrm{Cout}_{+3}=\begin{cases}1 & \text{if } \mathrm{Cout}_{+0}=0\\ \\ 2 & \text{if } \mathrm{Cout}_{+0}=1\end{cases} \quad (10)$$

Fig. 3(d). shows the $Cout_{+3}$ circuit. The threshold voltage of transistors T28, T29, T31 is normal, while the threshold voltage of the other transistors is such that the desired output is generated. The threshold voltage value of transistor T27 must be determined in order that the input value of $Cout_{+0}$ can be considered equal to logic one, two or three.

The threshold voltage of transistor T30 is in a way that the input value of $Cout_{+0}$ can be considered as logic zero or one. The threshold voltage value of transistor T32 must be determined in order that the input value of $Cout_{+0}$ is considered zero.

Finally, the outputs of all Sums and Couts are connected to the inputs of the e and f multiplexers. The circuit of both shapes is the same and only the input is different.

Fig. 3(e). shows the SUM final circuit. Threshold voltage of transistors T34, T35, T36, T39, T41, T43 is normal, while the threshold voltage of the rest of the available transistors is such that the desired output is generated. The threshold voltage value of transistor T33 is determined in order that the logic value of Cin input is considered to be three.

The threshold voltage value of transistor T37 is determined in a way that the input value of Cin can be considered equal to logic two or three.

The threshold voltage value of transistor T38 should be determined in order that the input value of Cin can be considered equal to logic zero, one or two. The threshold voltage value of transistor T40 is in a way that the input value of Cin can be considered equal to one, two and three. The threshold voltage value of transistor T42 should be determined in order that the input value of Cin can be considered equal to logic zero, one and finally the threshold voltage value of transistor T44 must be determined in order that the input logic value of Cin is only zero.

Fig. 3(f). shows the Cout final circuit. Threshold voltage of transistors T46, T47, T49, T51, T53, T55 is normal, while the threshold voltage of the rest of the available transistors is such that the desired output is generated. The threshold voltage value of transistor T45 is determined in order that the logic value of Cin input is considered to be three. The threshold voltage value of transistor T48 is determined in a way that the input value of Cin can be considered equal to logic two or three. The threshold voltage value of transistor T50 should be determined in order that the input value of Cin can be considered equal to logic zero, one or two. The threshold voltage value of transistor T52 is in a way that the input value of Cin can be considered equal to one, two or three. The threshold voltage of transistor T54 should be determined in order that the input value of Cin can be considered equal to logic zero, one and finally the threshold voltage value of transistor T56 must be determined in order that the input logic value of Cin is only zero.

All the $Cout_{+i}$ values are inputs of C_{out} 1-to-4 multiplexer, which is the final carry output. The inexact values in Cout blocks of all QFAs are negligible, while transistors are substantial- ly fewer, enhancing the performance of the circuit. The results are provided in the simulation section.

RESULTS & DISCUSSIONS

The complete simulation of the proposed scheme has been done using Synopsys HSPICE software. The QFA cells introduced in [26-30] were exact and were used to comparatively evaluate the proposed AQFA. The 32nm library models introduced in [23, 24] were employed to simulate the CNFET-based circuits. This model was developed for MOSFET-like SWCNFETs. Table 4 describes the important parameters of the model. This study introduced all possible inputs to the model to calculate the delay.

Finally, the longest delay would be assumed to be the delay of the circuit based on the critical path. The total power consumption is the average absorbed power of the transistors calculated over a long period. Although some inputs may not change the values of the output nodes, they can change internal nodes, leading to power consumption. As a result, an input pattern with all possible inputs confirms that the measured average power consumption is an estimate of the power consumption in the circuit. The PDP

Table 4. CNTFET model parameters.

Parameters	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	Mean free path in the intrinsic CNT channel	100 nm
L_{ss}	Length of doped CNT source-side extension region	32 nm
L_{dd}	Length of doped CNT drain-side extension region	32 nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	40 pF/m
Efi	The Fermi level of the doped S/D tube	6 eV

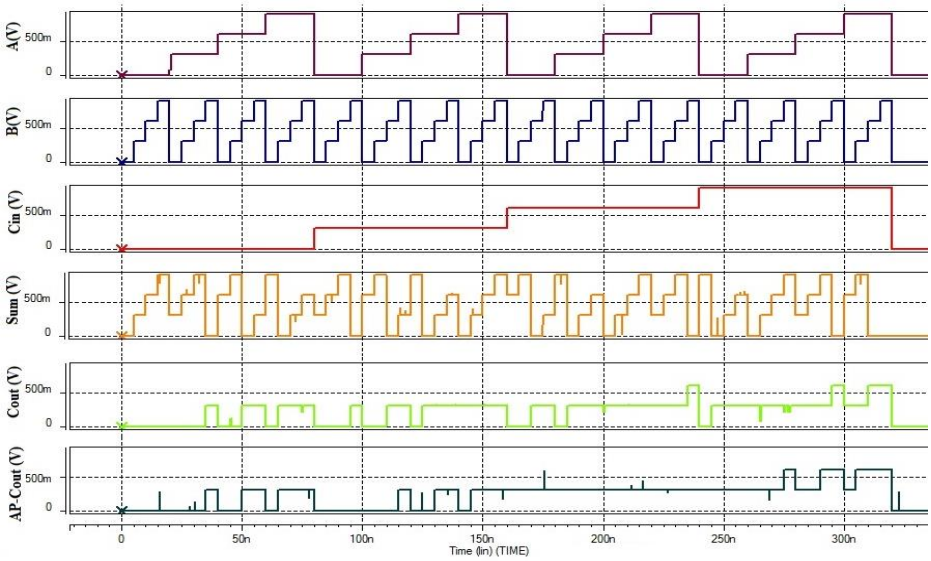

Fig. 4. Output and input waveforms for the proposed AQFA cell.

Table 5. Comparison of the proposed AQFA to other QFAs.

QFAs	Number of Device	Delay (ps)	Power Consumption (μW)	PDP (aJ)	EDP (E-25J.s)
Proposed AQFA	102	31.72	1.097	34.796	0.011
Design of [26]	135	54.49	6.324	344.59	0.187
Design of [27]	184	141.8	6.789	962.68	1.364
Design of [28]	287	63.24	8.972	567.38	0.358
Design of [29]	160	131.0	0.215	28.165	0.393
Design of [30]	157	49.83	1.608	80.130	0.039

is the product of the maximum delay and power consumption. And the EDP is obtained from the product of the PDP in the maximum delay.

Fig. 4 shows the pattern of the input and output waveforms for the proposed AQFA cell at room temperature, which represents the full performance for the exact Sum, Cout and approximate Cout. The simulations were carried out for a voltage supply of 0.9 V and a capacitance of 0.7fF at room temperature.

According to Table 5, the proposed model had a lower delay than the other models, due to the reduction of the critical data path. It was found that the proposed model had lower power consumption and a substantially lower PDP than the other CNTFET-based QFAs. These advantages mostly stemmed from fewer transistors, a simpler structure, and a shorter critical path. The excitability of a circuit is represented by the charging/discharging rates of the output capacitor of the circuit. Thus, sufficient power should remain to excite the remaining part of the circuit. Hence, different circuits are compared at different load capacitances.

Fig. 5 depicts the simulation results for a voltage supply of 0.9 V at room temperature. As can be seen, the proposed model had a satisfactory effect on the outputs compared to the other models.

Temperature variations are a major concern for circuit designers as they would negatively impact the performance of circuits. Thus, the circuits were simulated at different temperature for a voltage supply of 0.9V and a load capacitance of 2.1fF as shown in Fig. 6 As can be seen, the proposed circuit showed satisfactory performance at different temperatures.

The ability of the truth operation to function at different frequencies is a recent requirement

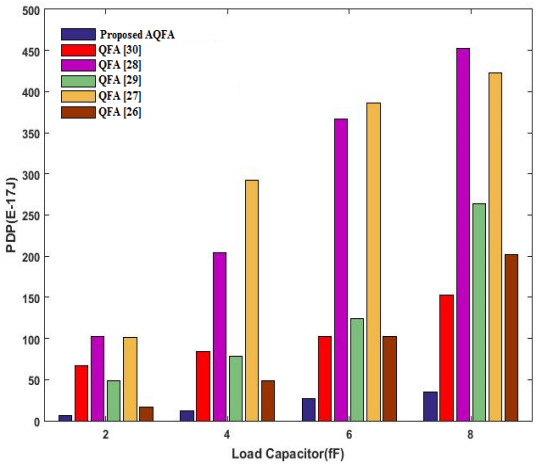

Fig. 5. PDP of the QFAs at different load capacitances.

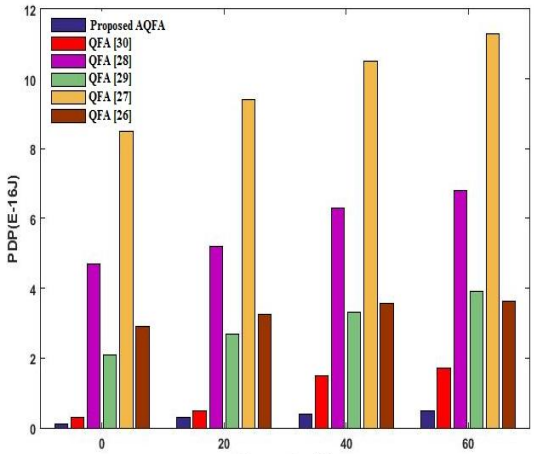

Fig. 6. PDP of the QFAs at different temperatures.

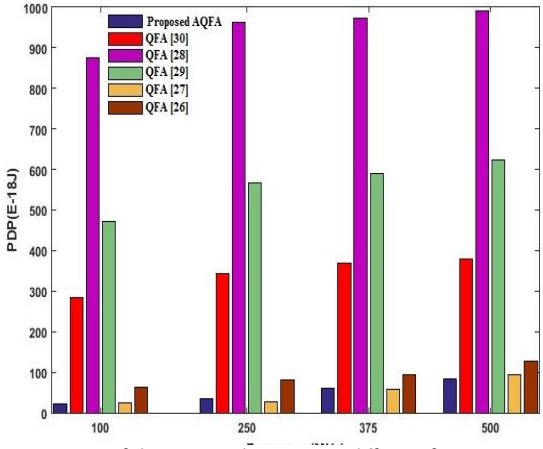

Fig. 7. PDP of the QFAs with respect to different frequencies.

of digital systems. Thus, the proposed and other designs were simulated at different frequencies. The results of these simulations are depicted in Fig. 7 These results were obtained with 0.9V power supply, room temperature, 2.1fF load capacitor, and the specified range of frequencies. According to this diagram, it is evident that PDP is lower in the proposed approximate full adder compared to the other designs.

CONCLUSION

This paper proposed a CNTFET-based AQFA as an emerging structure. The proposed circuit consisted of pass transistors and transmission gates. Approximate techniques are used in fault-tolerant applications, along with CNTFET transistors with lower power consumption and higher speed than MOSFET transistors. This improves the performance of specific processors, such as DSPs. In addition, due to the importance of adders in DSPs, researchers have sought to develop more optimal DSP designs. It was found that the proposed AQFA represents substantially lower delay and power consumption than the exact QFAs, mostly because of fewer transistors. Finally, it is observed that the proposed circuit by this model is smaller than the generated ones with other models.

CONFLICTS OF INTEREST

The authors do not have any conflicts of interest.

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